89600661

A

CONTROL DATA
CORPORATION

CDC® CARTRIDGE DISK DRIVE CONTROLLER

FA111-A

GENERAL DESCRIPTION
PROGRAMMING
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
LOGIC DESCRIPTION
MAINTENANCE
DIAGRAMS
MICRO PROGRAM LISTING

HARDWARE REFERENCE/MAINTENANCE MANUAL

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REVISION RECORD

REVISION	DESCRIPTION
01	Preliminary released.
(6/77)	
A	Manual released. This printing obsoletes all previous editions.
(10/77)	

Publication No.
89600661

REVISION LETTERS I, O, Q AND X ARE NOT USED

Address comments concerning this manual to:

Control Data Corporation
Publications and Graphics Division
4455 Eastgate Mall
LaJolla, Calif. 92037
or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
FA111-A	01	ECO CK1675	

LIST OF EFFECTIVE PAGES

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

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PREFACE

This manual describes the CDC® Cartridge Disk Drive Controller (CDDC). This controller interfaces to the CDC BR704-A & -B Cartridge Disk Drives. The CDDs must include the optional power supply, the daisy-chain option and use cartridges with 29 sectors per track.

The following documents may be useful as references:

Description	Publication No.
Microprocessor Reference Manual	88973500
1700 Computer System	60153100
Basic Micro-Programmable Processor Hardware Maintenance Manual	39451400
FA111-A Field Print Package	89600270
Operational Diagnostic System (ODS) Version 1 Reference Manual	39452100
Cyber 18-20/30 Timeshare Computer System Hardware Maintenance Manual, volumes 1 and 2	96769302

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GENERAL DESCRIPTION 1

INTRODUCTION

The Cartridge Disk Drive Controller (CDDC) contains the logic that interprets the CYBER 18 CPU function codes, controls the CDD operation, assembles and disassembles the 16-bit words between the CPU and the CDD and provides the CDD status information to the CPU. Communication between the Controller and the CPU is via the A/Q channel for status, control information and test and via the DMA channel for data transfer.

The CDDC uses the concept of micro-programming. It consists of TTL logic components mounted on one CYBER 18 11 in. by 13.7 in. (279.4 mm by 348 mm) board occupies one AQ/DMA slot in the CYBER 18 mainframe.

The CDDC has these additional characteristics:

1) Provides interface control for up to four CDD's connected in daisy-chain fashion. A single cable will connect the controller with the first CDD and each CDD has two identical interconnection plugs to enable the daisy-chain configurations.
2) The CDDC can handle any combination BR704 A and B CDD's all operating at 2400 RPM.
3) Provides autoload capability to the CYBER 18 processor from any one of the CDD's.
4) Allows dual CPU access to the CDD's with the disk relay station.
5) Provides maintenance capability, off line to any one of the CDD's.
6) Contains Track Offset capability for data retrieval from cartridges having misaligned tracks or disk imperfections.
7) Has the capability of 4 self tests for checking:
    1. Internal data paths and ALU.
    2. Internal FF's and jump conditions.
    3. Reading data via the DMA channel and the transmission of data via the A/Q channel.
    4. The A/Q channel data path.

Transfer Rate:	.4 Usec per bit (2.5 megabits per sec)
	6.4 Usec per 16-bit word (156 Kwords/sec)
Power	+5V at 9 amps/45 watts
Temperature	40^{o}F to 120^{o}F (4^{o}C to 49^{o}C)
Humidity	10 to 90 percent relative humidity with no condensation.
Warm Up time	None
Non Operating Environment	
Temperature	-30^{o}F to 150^{o}F (-22^{o}C to 65^{o}C)
Humidity	5 to 95 percent relative humidity with no condensation.

Figures 1-1 and 1-2 show possible CDDC/CDD configurations.

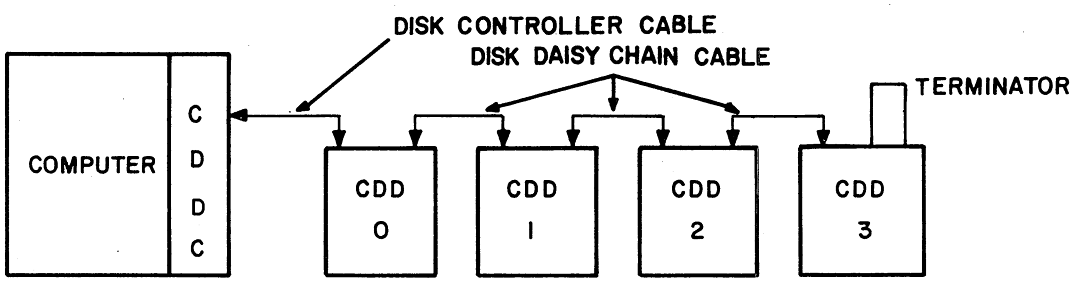


FIGURE 1 - 1: SINGLE COMPUTER ACCESS

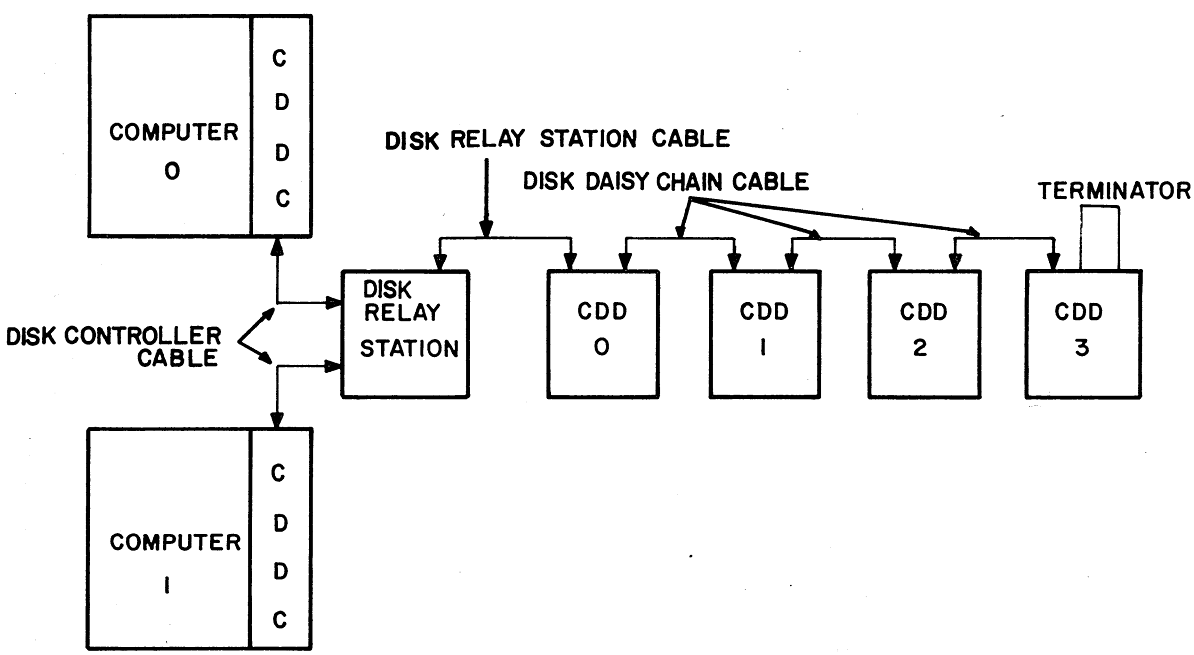


FIGURE 1 - 2: DUAL COMPUTER ACCESS

DISK ORGANIZATION

Addressing of the records is under program control from the CPU. Records within the file (disk) are accessed by Address Words sent from the computer. The Address Words are divided into four parts: the sector, disk, surface and cylinder.

The file, disk, cylinder, track and sector are defined as follows:

File - The file is defined as the entire recording surface available in the CDD unit.

Disk - The disk is defined as the entire recording surface on both sides of one disk, either the cartridge disk or the fixed disk.

Cylinder - The cylinder is defined as the recording surface on both surfaces of the cartridge and fixed disk at a given position of the head positioner.

Track - The track is defined as the recording surfaces under one read/write head at a given cylinder position.

Sector - The sector is defined as one data record and is the smallest addressable section of the file. The sector is 1/29th of a track and contains 1536 data bits or 96 sixteen-bit data words. It includes Head Gaps and Sync Patterns in order to synchronize the data between the drive and the controller.

SECTOR FORMAT

The total sector length is 2155 bits of which 1536 bits are data. Bit assignments are as indicated in Figure 1-3.

Head Gap 1	Sync. Pattern	Address	Checkword	Head G Gap 2	Sync Pattern	Data	Check Word	Tolerance Gap
120 Bits	112 Bits	24 Bits	12 Bits	120 Bits	112 Bits	1536 Bits	12 Bits	107 Bits

Figure 1-3. Sector Format

The head gap is required to allow the current to stabilize after turning on the read/write heads. The sync patterns are written as zeroes except for the last significant bit which is a 1. This bit denotes the end of the pattern. The Sync pattern enables the controller to recognize the start of serial bits from the drive. The 24-bit Address Format is shown in Figure 1-4. The controller generates and writes a checkword at the end of each address written and at the end of each data record. The checkword is used during Read to verify the accuracy of the data written. If the data-checkword does not agree with that which was written, the Checkword Error status will be set.

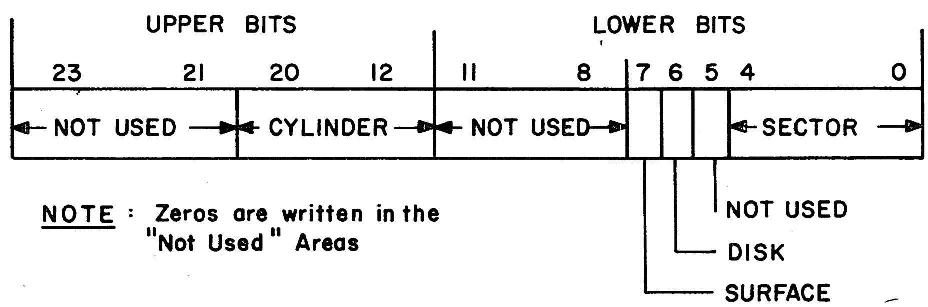


FIGURE 1-4. DISK ADDRESS FORMAT

DISK CHARACTERISTICS

Data Format:
16 bits per word
96 words per sector
29 sectors per track
2 tracks per cylinder
BR704-A Single Density CDD - 203 cylinders per disk
BR704-A Double Density CDD - 406 cylinders per disk
1 (or 2) disks per file

Data capacity:

1,536 bits per sector	(96 words per sector)
44,544 bits per track	(2,784 words per track)
89,088 bits per cylinder	(5,568 words per cylinder)
BR704-A Single Density CDD - 18,084,864 bits per disk	(1,130,304 words per disk)
BR704-A Double Density CDD - 36,169,728 bits per disk	(2,260,608 words per disk)
BR704-A Single Density CDD - 36,169,728 bits per file (max.)	(2,260,608 words per file)
BR704-A Double Density CDD - 72,339,456 bits per file (max.)	(4,521,216 words per file)

The CDDC communicates with the CPU via the AQ and DMA channels.

The Q register designates the equipment to be referenced and specifies the operation to be performed upon execution of the Input or Output instruction. Figure 2-1 illustrates the format of the Q register.

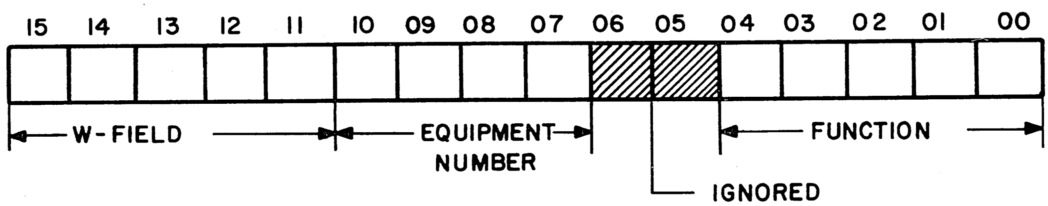


Figure 2-1. Q Register Format for I/O Instructions

The W field (bits 15-11) must always be zero.

The Equipment Field (bits 10-07) selects the CDDC. These bits must match the equipment number setting of the CDDC. The equipment number is determined by jumper plugs on the CDDC assembly.

Bits 05 and 06 are ignored by the CDDC.

Bits 04-00 specify the function to be performed by the controller in response to an Input or Output instruction.

The Output and Input function codes and commands are given in table 2-1 and 2-2, respectively.

Table 2-1: OUTPUT FUNCTIONS AND COMMAND CODES

Q_4	Q_3	Q_2	Q_1	Q_0	FUNCTION NAME
1	∅	∅	∅	∅	CLEAR CONTROLLER
0	0	0	0	0	ILLEGAL (REJECT)
0	0	0	0	1	DIRECTOR FUNCTION*
0	0	0	1	0	FIRST WORD ADDRESS
0	0	0	1	1	MEMORY BANK SELECT
0	0	1	0	0	LOAD FILE ADDRESS
0	0	1	0	1	WAIT FOR SEEK CHANGE
0	0	1	1	0	UNIT SELECT
0	0	1	1	1	BLOCK LENGTH
0	1	0	0	0	BUS CONNECT
0	1	0	0	1	INTERRUPT REQUEST
0	1	0	1	0	SEEK TO DEVICE
0	1	0	1	1	LOAD DISK ADDRESS
0	1	1	0	0	SELF-TEST 1
0	1	1	0	1	SELF-TEST 2
0	1	1	1	0	SELF-TEST 3
0	1	1	1	1	SELF-TEST 4

∅ can be either 1 or 0

* - see Table 2-2 for description

TABLE 2-2. OUTPUT FUNCTIONS FOR Q04-Q00 = 00001

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00	FUNCTION NAME
								0	0	1	0	0	0	0	0	RTZS
SURF	DISK	0	←	S E	C T	O R	→	TRK OFFS	0	0	0	1	0	0	1	READ DATA
SURF	DISK	0	←	S E	C T	O R	→	0	0	0	0	1	0	1	0	WRITE DATA
SURF	DISK	0	←	S E	C T	O R	→	TRK OFFS	0	0	0	1	0	1	1	COMPARE DATA
SURF	DISK	0	←	S E	C T	O R	→	TRK OFFS	0	0	0	1	1	0	0	CHECKWORD CHECK
SURF	DISK	0	0	0	0	0	0	0	0	0	0	1	1	0	1	WRITE ADDRESS
SURF	DISK	0	0	0	0	0	0	TRK OFFS	0	0	0	1	1	1	0	SENSE-VERIFY
								Ø	Ø	Ø	Ø	1	1	1	1	* ILLEGAL

*Reply is generated by No Operation performed.

TABLE 2-3. INPUT FUNCTIONS AND COMMAND CODES

Q_4	Q_3	Q_2	Q_1	Q_0	FUNCTION NAME
1	Ø	Ø	Ø	Ø	DYNAMIC STATUS 2-28
0	0	0	0	0	ILLEGAL (REJECT)
0	0	0	0	1	A-OUT STATUS
0	0	0	1	0	CURRENT WORD STATUS
0	0	0	1	1	CURRENT MEMORY BANK STATUS
0	0	1	0	0	FILE STATUS 2-34
0	0	1	0	1	SEEK COMPLETE STATUS
0	0	1	1	0	* ILLEGAL
0	0	1	1	1	* ILLEGAL
0	1	0	0	0	* ILLEGAL
0	1	0	0	1	* ILLEGAL
0	1	0	1	0	* ILLEGAL
0	1	0	1	1	* ILLEGAL
0	1	1	0	0	* ILLEGAL
0	1	1	0	1	* ILLEGAL
0	1	1	1	0	* ILLEGAL
0	1	1	1	1	* ILLEGAL

* The CDDC will reply to these functions; A-lines data, however, will be not valid.

Ø can be either 1 or 0.

OUTPUT FROM A OPERATIONS

All operations initiated by an OUTPUT instruction with the exception of Clear Controller, are rejected if a protect fault is detected or if the controller is busy. Clear Controller is rejected only due to a protect fault.

Excess noise on the A/Q channel may cause valid operations to be rejected.

Interrupt Request

The Interrupt Request command is used for enabling EOP, Alarm and/or Alternate CPU Bus Request interrupts and for clearing the interrupt response. Figure 2-2 illustrates the A Register Format.
The Interrupt Request command allows the CPU to select the conditions under which the interrupt response (signal) will become active.
This command will be rejected when the controller is busy or a protect fault occurs. The controller will not become busy upon acceptance of this command. The conditions for interrupt selected in the interrupt request command will remain valid for all subsequent instructions. MC, Clear Controller and Clear Interrupts will deselect all interrupts and will deactivate the interrupt response.

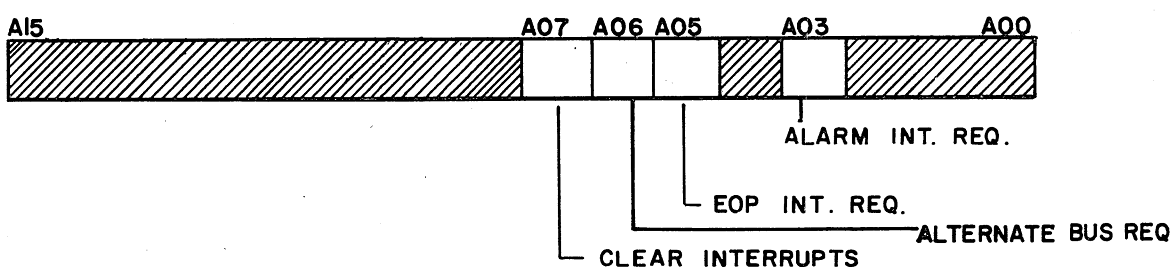


Figure 2-2. Interrupt Request A-Register Format

Clear Interrupts

A07 = 1 clears EOP and Alarm Interrupt Request Status and response.

Interrupt Requests may be cleared and enabled in the same Interrupt Request command. The order of execution is to first clear both interrupt requests and then enable interrupts according to bits A06, A05 and A03.

MC and Clear Controller clear all interrupt requests and response. Bits A00 - A02, A04, A08 - A15 are ignored by the Controller. A07 = 0 will cause no change in interrupt enable.

EOP Interrupt Request

A05 = 1: enables EOP Interrupt. An EOP Interrupt will be generated upon completion of an operation which caused the controller to go busy. An interrupt will become active approximately 2 microseconds before EOP Status is set. The following operations will generate an EOP interrupt provided EOP interrupt was requested.

1. READ DATA
2. WRITE DATA
3. COMPARE DATA
4. CHECKWORD CHECK
5. WRITE ADDRESS
6. SENSE - VERIFY
7. WAIT FOR SEEK CHANGE
8. UNIT SELECT
9. BUS CONNECT
10. SEEK TO DEVICE
11. SELF-TEST 1
12. SELF-TEST 2
13. SELF-TEST 3
14. SELF-TEST 4

Once enabled in the Interrupt Request command, interrupts will remain enabled for all subsequent instructions until disabled by Clear Interrupts, Clear Controller or MC.

A05 = 0: causes no change in EOP interrupt enable.

Alarm Interrupt Request

A03 = 1: enables an alarm interrupt to be generated whenever an alarm condition is detected. The interrupt will be sent 2 microseconds before the EOP status bit is set, regardless of when the alarm status bit becomes set. Once enabled by the Interrupt Request command, alarm interrupt will be enabled for all subsequent instructions, until disabled by Clear Interrupts, Clear Controller or MC.
A03 = 0: causes no change in Alarm Interrupt Enable.

Alternate Bus Request Interrupt

This interrupt is used for dual access to the CDDC/Controller bus. A6 = 1 allows an interrupt to be generated when the CDDC is "on bus" and not busy and the alternate controller is sending a bus request.

Bus Connect

The Disk Drives are capable of being shared by two CDDC's on a common bus. Whenever a CDDC wants to reference the Drive, it must first establish exclusive control of the Drive/Controller bus. The bus connect command is used for this purpose. Figure 2-3 shows the A-register format.

The Bus Connect command is rejected if the controller is busy or a protect fault occurs. If the command is accepted, the CDDC will become busy until bus control is established.

When the CDDC is off-bus (bus control has not been establised) and not busy the following commands will be rejected:

1. Director Function
2. Unit Select
3. Wait for Seek Change
4. Seek to Device

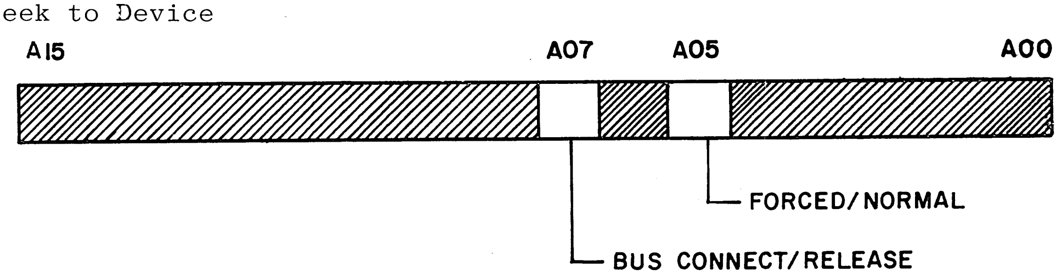


Figure 2-3. A Register Format for Bus Connect

Bus Connect/Release

A07 = 1: Instructs the CDDC to establish bus control. The CDDC will be busy until bus control is established. The mode of the connect is determined by A5.

A07 = 0: Instruct the CDDC to release the bus so that it may be available to the alternate controller. The controller will not go busy for bus release. MC will cause bus release. Clear Controller does not affect "On Bus" condition.

Bus Connect Request

The Bus Connect command has two modes of operation. These are valid only if A07 = 1.

1. Normal Request (A05 = 0)

   The CDDC will first check bus usage. If the bus in use by the alternate Controller, the CDDC will raise a flag (Bus Need) to the alternate Controller to notify the alternate that it requires the bus. It will then wait for the alternate to release the bus. During this time, the CDDC requiring the bus will be busy. When the bus does become available, the CDDC will gain control and will notify its CPU by setting On Bus status and by generating EOP status and EOP interrupt (providing EOP interrupt was selected).

2. Force Release (A05 = 1)

   The CDDC which requires the bus will send a Bus Force signal to the alternate Controller. This signal has the same effect on the alternate as a Master Clear and will cause the alternate to release the bus immediately. In addition to the Bus Force (Master Clear), the CDDC will send a forced release status signal to the alternate. This signal will allow the alternate to differentiate a Bus Force signal from a true Master Clear signal and thus, notify the alternate CPU that a bus relinquish took place. Having forced the alternate off the bus, the CDDC will gain bus control and will notify the CPU of this condition in the same way as for a normal request.

   Once bus control has been established, the CDDC which is "On Bus" may be obliged to relinquish the bus in response to a Bus Force signal from the alternate. Relinquishing of the bus causes the Alarm status bit and Bus Relinquish status (bit 7 of the Alarm Status word) to become active. An Alarm Interrupt will also be generated provided that Alarm Interrupt was selected.

A Force release signal from the alternate has the same effect on the CDDC as a Master Clear with the exception that interrupt requests are not affected by this signal.

Unit Select

The Unit Select command is used to select one of the four CDD's. Figure 2-4 shows the A-register format.

Unit Select commands will be rejected if the controller is off bus, a protect fault is detected, or the controller is busy.

NOTE: After the acceptance of the Unit Select Command the controller will become busy for the duration of the Unit Select operation.

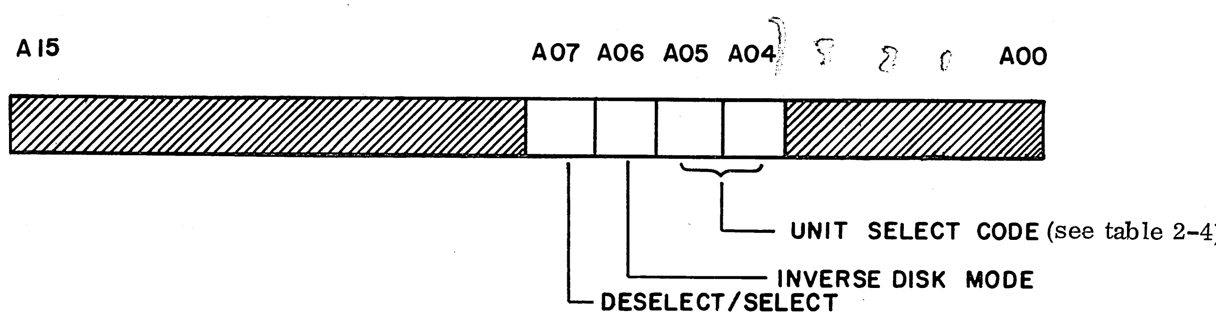


Figure 2-4. A-Register Format for Unit Select

A07 = 1: Instructs the CDDC to select the unit. Refer to unit select code (A05, A04).

A07 = 0: Instructs the CDDC to deselect the unit. A4 and A5 have no meaning for deselect. The Controller will not go busy for bus release.

A06 = 1: Instructs the CDDC to logically reverse the fixed and removable disks.

A06 = 0: Instructs the CDDC to work with the disks in the normal mode.

NOTES: a) Two units cannot be selected simultaneously. In case of selecting a second unit, the first unit will be automatically deselected.

b) Once the disks are reversed by A06 = 1, all subsequent CPU commands pertaining to disk selection will be reversed automatically by the controller.

c) Normal operation is re-established by providing a Unit Select function with A06 = 0.

d) If the Controller is in the inverse disk mode, the disk status bit will reflect the requested disk, although the actual (physical) disk status will be the inverse of that which is specified by this disk status bit.

TABLE 2-4. UNIT SELECT CODES

A05	A04	CODE
1	1	Unit 3
1	0	Unit 2
0	1	Unit 1
0	0	Unit 0

First Word Address

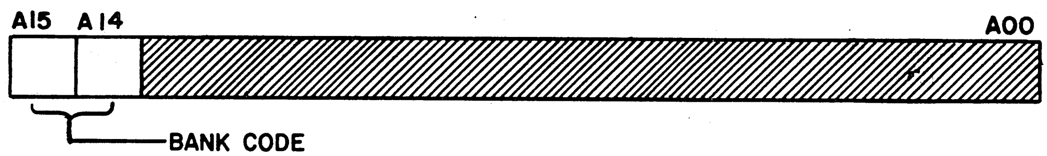
The first Word Address command specifies the address within a 65K memory bank of the first word of data to be transferred. "A" register bits 0-15 specify the address.

This command will be rejected if a protect fault occurs, or if the controller is busy.

Memory Bank Select

The Bank Select command specifies one of four 65K memory banks in which the address of the first word is to be found. The code is contained in A14 and A15. Figure 2-5 shows the A-register format.

Bank Select and First Word Address together provide an 18 bit address allowing the first word of the data transfer to be located within 256K of memory. The Bank Select command will be rejected if the controller is busy, or a protect fault occurred.



A_{15}	A_{14}	SELECTED BANK
0	0	BANK 0
0	1	BANK 1
1	0	BANK 2
1	1	BANK 3

Figure 2-5: BANK SELECT A-REGISTER FORMAT

Block Length

The Block Length instruction specifies the length of the buffer to be transferred starting at the first word address. Bits 0-15 of the A-register are used to specify a maximum block length of 65K.

Memory Bank Boundaries may be crossed during data transfers.

This command is rejected if the controller is busy, or a protect fault occurs.

Seek to Device

The Seek to Device command strobes the cylinder address from the A-register into the controller and initiates the head positioning motion in the CDD.

This function is rejected if a protect fault occurs, if the controller is busy, if it is not on-bus, not ready or is not on cylinder.

The On-Cylinder and seek complete status bits in the selected unit are cleared when the controller initiates the Seek operation and remains clear until the cylinder positioner reaches its new position.

NOTE: The controller goes busy just long enough to initiate the Seek command and then goes not busy, thus allowing overlap - seek operations on the four CDD's.

Care should be taken to ensure that the selected cylinder addresses are between 0 to 202 for single density CDD's or 0 to 405 for double density CDD's, otherwise a Drive Seek Error will occur.

Refer to Figure 2-6 for the bit assignments in the Seek command. A04 is the least significant bit.

A15	A14	A13	A12	A 04	A 03	A02	A01	A00
0	0	0	← CYLINDER	ADDRESS →	0	0	0	0

Figure 2-6: SEEK COMMAND BIT ASSIGNMENTS

<u>Load Disk Address</u>

The Load Disk Address command loads the cylinder address from the A register into the Cylinder Address Register in the controller and provides the controller with the starting cylinder address for all subsequent read/write Operations. This function is used for reloading the Cylinder Address Register after performing overlap-seek operations. If single disk operation is used, this command is not necessary since the Cylinder Address Register is loaded in the Seek to Device command.

This function is rejected if the controller is busy or a protect fault occurs.

Refer to Figure 2-6 for the A-register bit assignments.

Director Function Commands

The Director Function commands specify all of the CDD operations, with the exception of Seek to Device command. The function code is found on the A Lines.

Return to Zero Seek (RTZS)

This command recalibrates the selected drive and causes the heads of the selected disk unit to be positioned on cylinder zero. The RTZS function will clear the Drive Seek Error condition and the Alarm bit in the Dynamic Status.

This function will be rejected if the controller is busy, off-bus, not ready or if a protect fault occurs.

Figure 2-7 shows the A-register bit assignments for this function.

A 15 A08	A07	A06	A05	A04	A03	A02	A01	A00
	0	0	1	0	0	0	0	0

Figure 2-7. RTZS A-REGISTER BIT ASSIGNMENTS

Bits A00 to A04, A06 to A07 must be zero. Bit A05 must be 1.
Bits A08 to A15 can be as desired, either 1 or 0.

Write Data

The Write Data function directs the controller to transfer data from the computer memory to the CDD via the DMA channel. Data is read from the computer memory starting at the First Word Address and continues until the number of words specified in Block Length has been transferred. If the data transfer ends within a sector the controller fills the remainder of the sector with zeros and then writes the checkword. If the data transfer extends beyond the last sector of the "top" surface, the controller will automatically continue the transfer on the first sector of the bottom surface of the same cylinder. If the data transfer extends beyond the last sector in a cylinder, the controller will move the cylinder positioner to the next cylinder and continue the transfer there. If transfer is attempted beyond the last cylinder in a disk, an End of Medium error will occur. No switching from fixed to removable disk, or vice versa occurs.

Several abnormal conditions can develop during this operation. Detection of these abnormal conditions by the controller causes the operation to cease. These abnormal conditions are:

1. Device Seek Error
2. Unit becomes Not Ready
3. Unit becomes Not On Cylinder
4. Missing Index/Sector Pulse
5. Controller Seek Error
6. Wrong Sector Format
7. Wrong Device Transfer
8. Lost Data
9. DMA Address Error
10. DMA Parity Error
11. End of Medium
12. The Disk is Write Protected

Detection of any of these abnormal conditions causes the corresponding status bit and the alarm bit to set.

NOTE: During overlap-seek operation the Write Data, Read Data, Compare Data, Checkword Check or Write Address Function will be accepted if the controller and the selected unit are not busy. The controller's data path can be used only by one unit at a time.

Figure 2-8 shows the A-register bit assignment for the Write Data function.

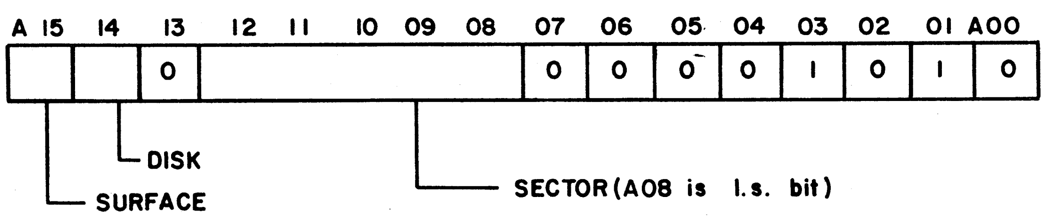


Figure 2-8: WRITE DATA A-REGISTER BIT ASSIGNMENTS

Bits A00, A02, A04 to A07 must always be zero.
Bits A01, A03 must be 1.
Bits A08 to A12 define the starting sector of the data to be written; the sector address should be in the range 0 to 28.
Bit A13 must always be zero.
Bit A15 defines the disk surface:

0 = top surface
1 = bottom surface

Bit A14 defines either the fixed or removable disk.

0 = removable disk
1 = fixed disk

The controller will reject this function if it is busy, off-bus, not ready, or a protect violation occurs.

The controller becomes busy upon the acceptance of this function and remains busy until the end of the last sector operated on. The EOP status is set 1 μsec after the BUSY status is cleared.

<u>Read Data</u>

The Read Data function directs the controller to transfer data from disk file memory to computer storage. The method for obtaining the starting addresses and the buffer length is the same as for the Write Data function. If data transfer to the computer stops within a sector, the controller continues reading the data until the end of the sector and determines if the checkword is correct. If the data transfer extends beyond the last sector of the "top" surface, the controller will automatically continue the transfer from the first sector of the "bottom" surface. If data transfer extends beyond the last sector in a cylinder, the controller moves the cylinder positioner to the next cylinder and continues the transfer there. If transfer is attempted beyond the last cylinder in a disk an End of Medium error will occur.

Several abnormal conditions can develop during this operation. Detection of these conditions by the controller causes the operation to end. The abnormal conditions are:

1. Unit becomes Not ready
2. Unit becomes On Cylinder
3. Device Seek Error
4. Missing Index/Sector Pulse
5. Controller Seek Error
6. Wrong Sector Format
7. Wrong Device Transfer
8. Lost Data
9. DMA Address Error
10. DMA Protect Fault
11. DMA Parity Error
12. Checkword Error
13. End of Medium

Detection of any of the abnormal conditions causes the corresponding status bit and the Alarm bit to be set.

NOTES: See Notes in description of the Write Data section.

Figure 2-9 gives the A-register bit assignment for the Read Data command.

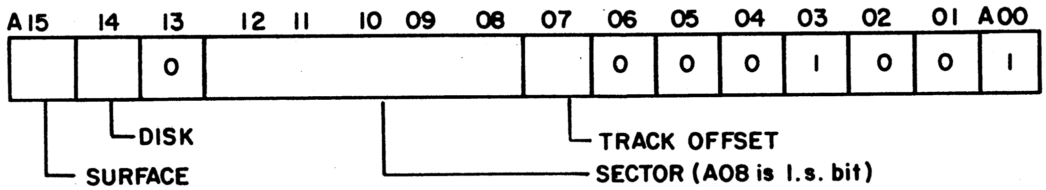


Figure 2-9. READ DATA A-REGISTER BIT ASSIGNMENTS

Bits A00, A03 must always be 1.
Bits A01, A02, A04 to A06 must always be zero.
Bit A07 is the track offset bit: it is used for data recovery operations. When this bit is set it causes the read heads in the disk to be displaced up to 1000 microinches from their normal position in an analog motion, and cycles at the rate of 500 msec. When not enabled the heads return to the nominal tracks position. This facilitates data retrieval from cartridges having misaligned tracks or disk imperfections.
Bits A08 to A12 define the starting sector of the data to be read; the sector address should be in the range of 0 to 28.
Bit A13 must always be zero.
Bit A15 defines the disk surface:
    0 = top surface
    1 = bottom surface
Bit A14 defines either the fixed or removable disk:
    0 = removable disk
    1 = fixed disk

The controller will reject this command if it is busy, off-bus, a protect violation occurs, or the unit is not ready.

The controller becomes Busy upon acceptance of this function and remains Busy until the end of the last sector operated on. The End of Operation is set 1 μsec after the Busy status is cleared.

Compare Data

The Computer Data function directs the controller to compare data from computer memory with data read from file storage. The method for obtaining the starting address and the buffer length is the same as that for the Write Data and Read Data operation. The comparison stops when the computer buffer limit is reached, but the controller will read until the end of the last sector compared to determine if the CRC is correct. If the data does not compare, the No Compare status bit will be set.

Several abnormal conditions can develop during this operation. Detection of these conditions by the controller causes the operation to end, but the controller continues to read until the end of the sector to determine if the CRC is correct. The abnormal conditions are:

1. Lost Data
2. DMA Address Error
3. Checkword Error
4. DMA Parity Error
5. End of Medium
6. Unit becomes Not Ready
7. Unit becomes Not On Cylinder
8. Device to Seek Error
9. Missing Ind/Sector Pulse
10. Controller Seek Error
11. Wrong Sector Format
12. Wrong Device Transfer
13. No Compare

Detection of any of the abnormal conditions causes the corresponding status bits and the Alarm bit to be set.

NOTES: See Notes in Write Data Section

Figure 2-10 shows the A-register bit assignments for the Compare Data Function.

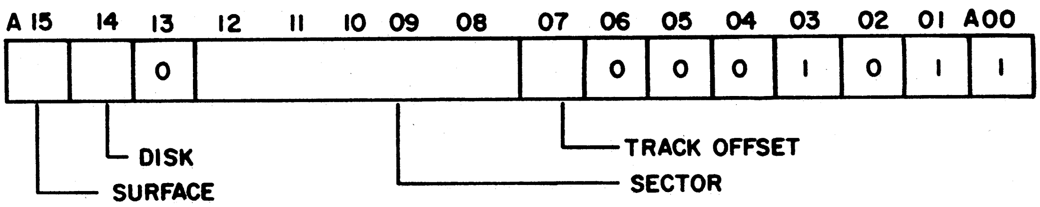


Figure 2-10. COMPARE DATA A-REGISTER BIT ASSIGNMENTS

Bits A00, A01, A03 must always be one.
Bits A02, A04 to A06 must always be zero.
Bit A07 is the track offset bit - see description in the Read Data section.
Bits A08 to A12 define the starting sector address should be in the range 0 to 28.
Bit A13 must always be zero.
Bit A15 defines the disk surface:

0 = top surface
1 = bottom surface

Bit A14 defines the fixed/removable disk:

0 = removable disk
1 = fixed disk

The controller will reject this command if it is busy, off-bus, a protect fault occurs, or the unit is not ready.

The controller becomes Busy upon acceptance of this function and remains Busy until the end of the last sector operated on. The End of Operation status is set one 1 μsec after the Busy status is cleared.

Checkword Check

The checkword Check function directs the Controller to read the data from the disk into the checkword logic to be checked until the number of words specified in the Block Length has been transferred (the Controller continues reading the data until the end of the sector).

The operation is the same as for Read Data command, except that no data is transferred to or from the computer memory.

The reject conditions are the same as for Read Data; the abnormal conditions which occur are also the same except for DMA Address/Protect Fault/Parity Errors which do not occur.

Figure 2-11 shows the A-register bit assignments for the Checkword Check command.

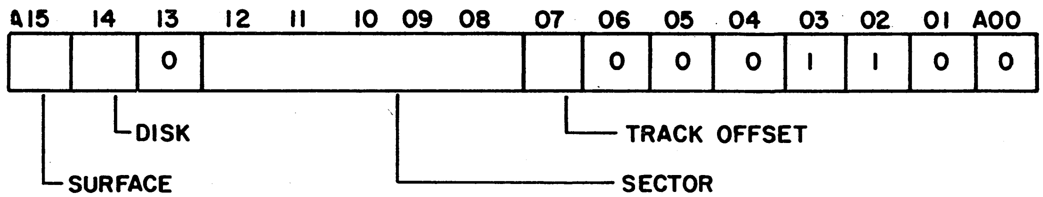


Figure 2-11: CHECKWORD CHECK COMMAND, A-REGISTER BIT ASSIGNMENTS

Refer to Read Data command for controller performance under abnormal conditions.

<u>Write Address</u>

The Write Address function causes the controller to write the address tags of all the sectors in the presently available track. The written track address is that specified by the Cylinder Address Register, and by the A15 and A14 A-Register Bits in Write Address command. No data is transferred to or from memory. The Address Tags (and the Address-Checkword) are written sequentially from 0 through 28_{10}, starting from the index mark.

Detection of abnormal condition (Not Ready, Not On Cylinder, Device Seek Error, Missing Index/Sector Pulse or Disk Write Protected) by the controller causes the operation to cease and the corresponding status bits in Alarm File Registers and the Alarm bit in Dynamic Status to be set. (See Note in WRITE DATA Section). This function is rejected if the controller is busy, off-bus, if a protect violation occurs or the unit is not ready.

Figure 2-12 shows the A-register bits for the Write Address function.

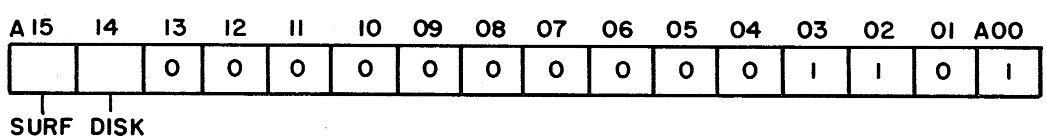


Figure 2-12: WRITE ADDRESS COMMAND A-REGISTER BIT ASSIGNMENT

Bits A00, A02, A03 must always be one.
Bits A01, A04 to A13 must always be zero.
Bits A14, A15 are Disk and Surface - see description in Write Data Section.

Sense Verify.

The Sense Verify command causes the controller to read the address of the sector currently under the read head, with CPU notification (EOP Interrupt) upon completion. The Controller compares the sensed track address with the one present in the Cylinder Address Register and generates Alarm and Controller Seek Error if a mismatch occurs.

The CPU may then read the contents of File Register "12 + 13" to retrieve the true sector address and File Register "14 + 15" to retrieve the true cylinder address.

Figure 2-13 shows the A-Register for this function.

A 15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	A 00
		0	0	0	0	0	0		0	0	0	1	1	1	0
SURF	DISK							TRACK OFFSET							

Figure 2-13. SENSE - VERIFY COMMAND A-REGISTER BIT ASSIGNMENTS

Bits A00, A04 to A06, A08 to A13 must always be zero.
Bits A01 to A03 must always be one.
Bits A07 is the track offset bit - see description in the Read Data Section.
Bits A14, A15 are Disk and Surface - see description in Read Data Section.

Detection of abnormal conditions (Not Ready, Not On Cylinder, Device Seek Error, Missing Sector Pulse or Wrong Sector Format) by the Controller, causes the operation to cease and the corresponding status bits in the Alarm File Registers and the Alarm Bit in the Dynamic Status to be set.

This function is rejected if the controller is busy, off-bus, a protect violation occurs, or the unit is not ready.

Clear Controller

The Clear Controller command clears controller status, registers, interrupt requests and responses. The A-register contents have no meaning for this command.

The following Dynamic Status bits are reset by Clear Controller or Master Clear (MC).

- Controller Busy (A01)
- Interrupt Response (A02)
- Alarm (A03)

Clear Controller and MC set EOP (A08).

All other Dynamic Status bits are not affected by Clear Controller.

Master Clear (MC) resets in addition the following Dynamic Status bits:

- Single Density (A07)
- On Bus (A12)
- Controller Protect (A14)

The Clear Controller command is rejected only if a protect fault occurs. Clear Controller does not affect the contents of the Register File. Clear Controller must be used with discretion, since it will stop any current operation.

Wait for Seek Change

This command allows Seek to be done in parallel (Overlap-Seek) with the CPU receiving notification (EOP Interrupt) on the completion of each Seek by detecting any change in Seek Complete status of the four units (i.e. unit which was previously not Seek Complete becoming Seek Complete, or vice versa). The Q register is loaded as per Table 2 - 1 and A-register bits 0 ÷ 3 specify the initial unit Seek Complete status (see Figure 2-14). Each bit corresponds to one of the units (A0 to unit 0, A1 to unit 1, A2 to unit 2, A3 to unit 3). Upon acceptance of this command the controller will become busy and will sample the Seek Complete status of each of the four units. The result of this sampling will then be compared with the unit Seek Complete status originally received from the CPU via the A-register.

The sample and compare operation will continue until the original Seek Complete status and the actual (sampled) Seek Complete status is not equal, indicating that one (or more) of the units which was previously not Seek Completed has become Seek Complete (or vice versa). EOP status and EOP interrupt (if requested) will be generated when a change in the Seek Complete status is detected. Upon completion of this command, the CPU should read Seek Complete status to determine which of the units completed its Seek operation.

Wait for Seek Change is rejected if the controller is off-bus, or if the controller is busy.

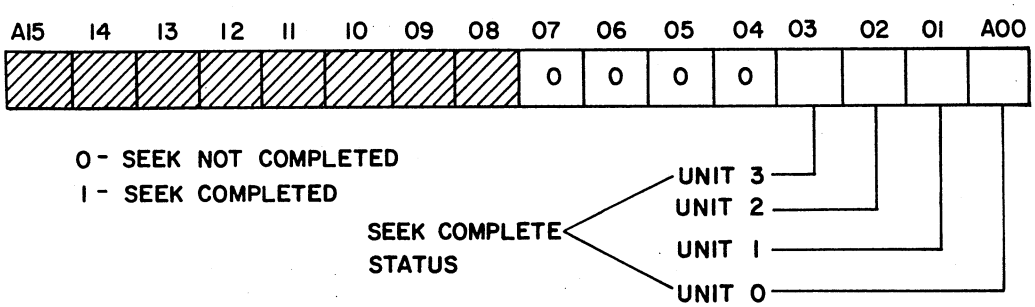


Figure 2-14: WAIT FOR SEEK CHANGE, A-REGISTER BIT ASSIGNMENTS

Load File Address

The Load File Address command specifies the address of a register in the 16 register file which will be read by a file register status request.

Bits A00 to A03 determine the file address, where A00 is the least significant bit.

The Load File Address command is rejected if the controller is busy or a protect fault is detected.

Self-Test 1

Self-Test 1 causes the CDDC to check its internal data paths and ALU. The lower 8 bits of the A-register specify the data which is to be transferred along the internal data paths of the CDDC. The upper and lower 8 bits of the A-register specify the data which is to be operated on by the ALU.

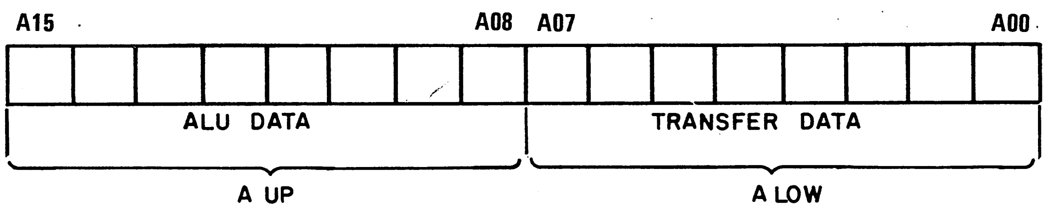


Figure 2-15. SELF TEST 1 A-REGISTER FORMAT.

Upon acceptance of this command, the CDDC will become busy and remain busy until the internal transfers and ALU operations are complete, after which Busy status will be reset and EOP status will be set 1 microsecond later.

If EOP status is not set within 2 milliseconds, this is an indication that the controller is defective.

After busy status is reset, A-Out Status should be read to determine the success of the test. The upper 8 bits of the A-register should contain F_{16} plus the dat that was originally sent in the lower 8 bits of the A-register in Self-Test 1. The lower 8 bits should contain an expected result which is a function of the data originally sent in the upper and lower 8 bits of the A register during Self-Test 1 according to the following equation:

$$A\ out\ low = ((((A\ up - 1) \times 2 + A\ Low + 1 - A\ up) \cdot A\ Low) \text{ or } A\ up)$$

Carry Out is disregarded.

Figure 2-16 illustrates the Self-Test 1 Result.

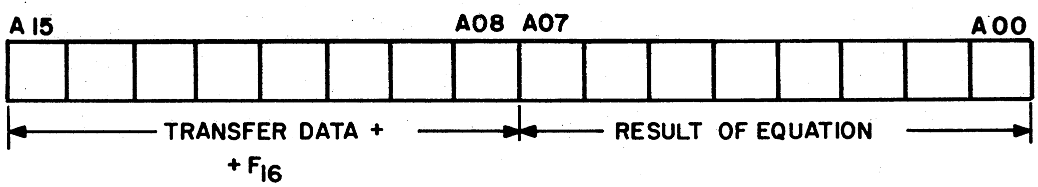


Figure 2-16: SELF-TEST 1 RESULT

Self-Test 1 will also load the 16 file register in the following way:

$$
\begin{aligned}
RAM\ (0) &= A_L + F_{16} \\
RAM\ (1) &= A_L \\
RAM\ (2) &= A_L + 1 \\
RAM\ (3) &= A_L + 2 \\
RAM\ (4) &= A_L + 3 \\
RAM\ (5) &= A_L + 4 \\
RAM\ (6) &= A_L + 5 \\
RAM\ (7) &= A_L + 6 \\
RAM\ (8) &= A_L + 7 \\
RAM\ (9) &= A_L + 8 \\
RAM(10) &= A_L + 9 \\
RAM(11) &= A_L + A_{16} \\
RAM(12) &= A_L + B_{16} \\
RAM(13) &= A_L + C_{16} \\
RAM(14) &= A_L + D_{16} \\
RAM(15) &= A_L + E_{16}
\end{aligned}
$$

This should be checked by loading the address and reading the contents (status) of each of the 16 file registers.

NOTE: See remarks common to all self tests.

Self-Test 2

Self-Test 2 checks the CDDC internal F/F's, jump conditions and Dynamic Status F/F's. The A-register is not used for this command. Upon acceptance of this command, the controller will become busy until the test is complete, after which Interrupt response is set, Busy status will be reset and EOP will be set one microsecond later. If EOP is not set after 2msec from the time that the controller becomes busy, this is an indication that the controller is defective.

Prior to the execution of Self-Test 2, a Clear Controller command should be issued to ensure that all Dynamic Status F/F's are in their quiescent state. Figures 2-17 and 2-18 illustrate the Dynamic Status after execution of Clear Controller and after execution of Self-Test 2, respectively.

				0	0		1					0	0	0	
A 15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	A 00

Figure 2-17. DYNAMIC STATUS AFTER CLEAR CONTROLLER

			0				1	1				1	1	0	
A 15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	A 00

Figure 2-18. DYNAMIC STATUS AFTER SELF-TEST 2

When the test is complete (busy status reset) A-Out Status should be read directly following the completion of the test to determine if the test was successful. A-Out Status $ACED_{16}$ indicates that the test was successful. A-Out Status $DEAD_{16}$ or any other status indicates that the controller is defective.

If A-Out Status gives the successful result ($ACED_{16}$) Dynamic Status should be read and compared to Figures 2-17 and 2-18. If these are not identical, the controller is defective. Self-Test 2 checks the interrupt request and consequently an EOP interrupt response will be generated regardless of whether an interrupt is requested.

Since after execution of Self-Test 2 the Dynamic Status does not indicate the true status of the controller, a Clear Controller command must be issued before performing any further operations. After Self-Test 2 the controller becomes off-bus (A12=0).

Self-Test 2 will be rejected if the controller is busy or a protect fault is detected (see remarks common to all tests).

Self-Test 3

Self-Test 3 checks the capability of the CDDC to read data via the DMA channel and transmit data via the A/Q channel. With the Q register loaded as per Table 2-1 and Figure 2-1, execution of an OUTPUT instruction will cause the CDDC to read one word from the memory at the location specified by the First Word Address and Memory Bank Select commands. The eighteen bit Memory Address composed of the Bank Select and First Word Address will be incremented by one after completion of the Self-Test 3. Upon acceptance of this command, the controller will become busy and remain busy until the operation is complete, after which Busy status will be reset and EOP status will be set one micro-second later.

After completion of this command, A-Out Status should be read. The A-Out Status should be compared with the original contents of the address specified by the Last Word Address and Bank Select. If those two are not identical, the controller is defective.

Self-Test 3 will be rejected if the controller is busy, or protect fault is detected (see remarks common to all Self-Tests).

Self-Test 4

Self-Test 4 checks the A/Q channel data path of the CDDC by reading one word via the A/Q channel and writing the same word via the DMA channel. With the Q register loaded as per Table 2-1 and Figure 2-1 execution of an output instruction will cause the CDDC to read the data contained in the A-register and then write it into memory at the address specified by the First Word Address and Memory Bank Select commands.

Upon acceptance of this command, the controller will become busy and remain busy until the transfer into memory is complete, after which Busy status will be reset and EOP status will be set one microsecond later. The CPU should then compare the word written into memory by the CDDC with the one originally sent via the A/Q. If they are not identical, the controller is defective.

(See remarks common to all Self-Tests)

Self-Test 4 will be rejected if the CDDC is busy or a protect fault is detected.

Remarks common to all Self-Tests:

a) Clear Controller must be performed before any test.
b) The CPU must read A-out status first and then read Dynamic Status.
c) The Self-Tests do not check Bank Select so it is recommended to load Bank Select with 0 and then to read it, after that to load Bank Select with 3 and then to read it.
d) Self-Tests do not affect Unit Select or Protect conditions.
e) Bus Release must be performed before any test.

INPUT TO A OPERATIONS

With the Q register loaded as per Table 2-3 and Figure 2-1, execution of an input instruction will cause the controller to load the A-register with the desired controller status. All status requests except Dynamic Status requests are rejected if the controller is busy. Excess noise on the A/Q channel may cause a valid status request to be rejected.

Dynamic Status

Figure 2-19 shows the A-register format for the Dynamic Status response; Dynamic Status requests are always accepted (even if the controller is busy).

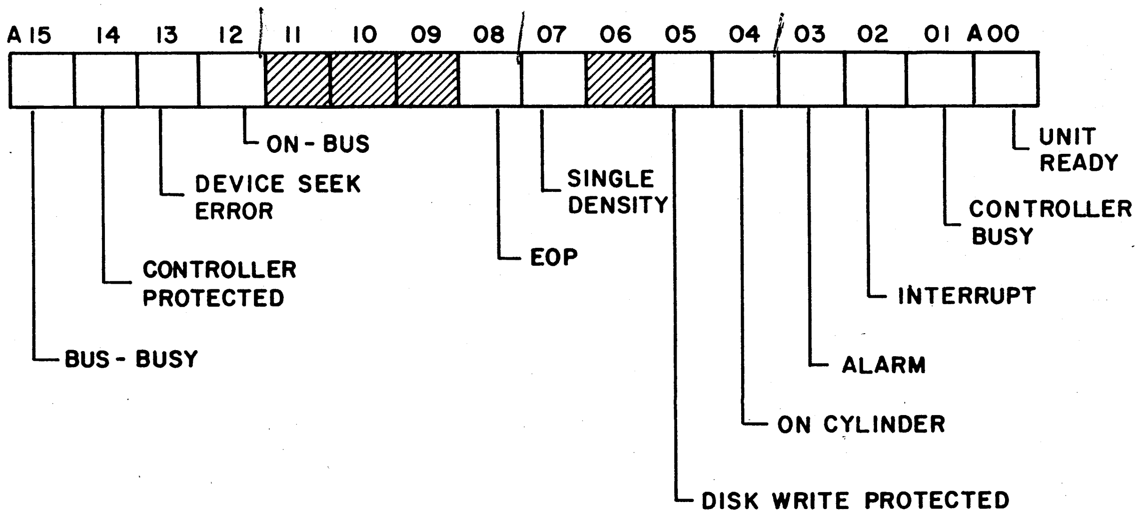


Figure 2-19. DYNAMIC STATUS A-REGISTER BIT ASSIGNMENTS

Unit Ready Bit (A00)

A00 = 1, the selected CDD is ready.

A00 = 0, the selected CDD is not ready.

Controller Busy (A01)

Upon acceptance of the following commands, A01 will be set, indicating that the controller is busy:

1. Unit Select
2. Bus Connect
3. Director Function (except RTZS Function)
4. All Test Modes
5. Wait for Seek Change
6. Seek to Device

All commands to the controller except Clear Controller and Dynamic Status request will be rejected when busy status is set.

Busy status, will be cleared upon completion of the command which caused the controller to become Busy. MC or Clear Controller will also clear Busy.

Interrupt Response (A02)

A02 = 1 indicates that the EOP, Alarm or Alternate Bus Request Interrupt response is active.
A02 is reset by Clear Interrupts (see Interrupt Request), Clear Controller and MC.

Disk Write Protected (A05)

This bit indicates that the unit's "WRITE PROTECT SWITCH" is on and all write functions are inhibited by the unit. The Controller will set Alarm in Write Data and Write Address commands whenever the disk is write protected, since they cannot be executed.

Single Density (A07)

When "one" this bit indicates that the selected CDD is a single density unit (203 tracks only). When "zero" this indicates that the selected CDD is a double density unit (406 tracks).

End-of-Operation (EOP) (A08)

EOP status set indicates that the previous operation has been completed.

EOP status will reset approximately 1 microsecond after busy status is set and will become set 1 microsecond after busy status is reset.

Since no new commands will be accepted by the controller when busy, EOP becoming set serves as a warning that the controller will finish its current operation.

The Interrupt Status A02 and the EOP Interrupt Response are available 2 microseconds before the EOP status is set.

On-Bus and Bus Busy (A12, A15)

On-Bus and Bus Busy status bits together determine the status and usage of the CDD/Controller bus according to the following table:

TABLE 2-5. DISK/CONTROLLER BUS STATUS

BUS BUSY	ON BUS	STATUS
0	0	The bus is not being used by either CDDC
0	1	This CDDC has control of the bus and can access the Disks
1	0	The other CDDC has control of the bus
1	1	This CDDC has control of the bus, and the other CDDC is sending an alternate Bus Request.

Unit Select, Seek to Device, Wait for Seek Change and Director Function commands will be rejected if On-Bus status is not set.

On-Bus status will be cleared upon:

1. Acceptance of a bus release command.
2. Bus Relinquish due to a forced request from the other CPU.
3. Master Clear MC.

Bus Busy will be reset upon release or relinquishment of the bus by the other controller.

Alarm (A03)

A03 will become active whenever an error occurs during a data transfer of conditions arise which require external intervention. File register "6+7" should be checked to determine the cause of the alarm. (Note: alarm status may be checked only after the controller goes not busy).

During Write Data operations the data transfer from main memory will be terminated immediately after the detection of the error, but the controller will fill the rest of the sector with zeroes. The controller will stay busy until the end of the sector.

During Read Data, Checkword Check and Compare Data operations the data transfer will be terminated immediately after the detection of the error. The controller will read the data from the disk until the end of the sector to determine if the CRC is correct. Alarm Status bit will become active at the time that the alarm condition occurs, but the Alarm Interrupt will be sent to the CPU when the controller goes Not Busy.

Alarm Status will reset upon the acceptance of any new command which causes the controller to become busy, or Clear Controller or MC.

This bit indicates that one of the following abnormal conditions has occurred (alarm sets immediately):

a. Device becomes Not Ready during a Director Function Operation
b. Checkword Error
c. Controller Seek Error
d. Lost Data
e. Drive Seek Error during Director Function Operation.
f. DMA Parity Error
g. DMA Protect Fault
h. Bus Relinquished
i. DMA Address Error
j. Compare Error
k. End of Medium
l. Missing Index/Sector Pulses
m. Wrong Sector Format
n. Wrong Device Transfer

o. No On Cylinder during Director Function operation.

p. Fault occurs during operation on CDD.

On Cylinder (A04)

This bit indicates when set that the heads have reached the desired cylinder and are ready to read, write or seek. On Cylinder will also be sent when a Seek Error has occurred.

Drive Seek Error (A13)

This bit indicates when set that the heads have moved to an illegal address or that a seek was not completed within 200 msec.

Alarm on Drive Seek Error arises only in Director Function operation, i.e. If Drive Seek Error was created in the previous See operation, the Alarm is set at the beginning of the function. Also Drive Seek Error could happen in passing of cylinders during Director Function operation.

Recalibration of the device by the RTZS command is mandatory when a Drive Seek Error Condition is detected by the CPU.

The RTZS clears the Seek Error condition

Controller Protected (A14)

When active indicates that a protected unit is selected. The controller will reject all unprotected OUTPUT instruction. Unprotected Status requests will be accepted.

Deselecting of the protected unit or selecting of a non protect unit will clear A14.

A-Out Status

A-Out Status is used for reading the results of the CDDC self-tests 1, 2 and 3, After execution of one of these self-tests, the result will reside only in the CDDC A-Out register. Since the A-Out register is also used for sending other data on the A-Lines, self-test results should be read directly following the execution of the self-test to ensure that the result is not lost. This request will be rejected if the Controller is busy.

In general, the A-Out register will contain the last status that was sent to the processor.

Current Memory Bank Status

The upper two bits of the A-register will be filled with the code of the Memory Bank that was last referenced.

This request will be rejected if the controller is busy.

For Read Data, Write Data, Compare Data operations the Current Memory Bank status is continuously updated as the data transfer progresses.

File Registers Statuses

File Status requests allow the contents of the CDDC internal 16 register file to be read. The file address is specified by the Load File Address Command. Since the File is 8 bits wide, two consecutive file words will be loaded into the A-register. The lower portion of the A-register will be loaded with the contents of the file at the address specified by the Load File Address command. The upper portion of the A-register will be loaded with the contents of the specified file address plus one.

Table 2-6 specifies the usage of the file registers. File registers status should be read immediately following the execution of the load File Address command to ensure that the loaded file address remains valid.

This request will be rejected if the Controller is busy.

Table 2-6. FILE USAGE

FILE REGISTER	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
REG "0+1" SECT, SURF, DISK	SURF	DISK	0	← SECTOR →												
REG "2+3" CYLINDER	0	0	0	← CYLINDER →									0	0	0	0
REG "4+5"																
REG "6+7" ALARM	0	0	BUS REL	WRNG D.TR	WRNG S.FM	MISS I/S	CONT S.ER.	END MED	0	0	COMP ERR.	CHW ERR	LOST DATA	DMA PA.E	DMA PR.F	DMA AD.E
REG "8+9" BLOCK LENGTH	← BLOCK LENGTH →															
REG "10+11" CHECKWORD	← CHECKWORD STATUS →															
REG "12+13" TRUE SECT SURF, DISK	TRUE SURF	TRUE DISK	0	← TRUE SECTOR →					0	INVRS DISK	0	0	0	0	0	0
REG "14+15" TRUE CYLINDER	0	0	0	← TRUE CYLINDER →									0	0	0	0

Cyl 15 → 7
Surface 6
Disk 5
Sect 4 → 0

"1" = lower
"1" = Fixed

Sector, Surface, Disk Status (File "0+1")

This status contains the sector, surface and disk information as received from the CPU and as updated during the operation for any Read Data, Write Data, Compare Data, Write Address and Checkword Check operations.
See Note in section "True Sector/Surface/Disk Status".

Cylinder Status (File (2"+3")

File "2+3" registers function as the Cylinder Address Register containing the cylinder address information as received from the CPU; this initial address information is updated by the controller as the disk operation progresses.

Alarm Status (File "6+7")

This is the Alarm Status information register which contains the alarm status bits (except for Device Seek Error, Not Ready, Not On-Cylinder bits which are found in the Dynamic Status).

Contents of the Alarm Status register is valid only when the "Alarm" bit is set in the Dynamic Status word.

DMA Address Error (A00)

A00 will be set if an attempt is made to reference a non-existent Memory stack.

DMA Protect Fault (A01)

A01 will be set if a data transfer initiated by an unprotected instruction attempts to write Data into a protected area of memory. The original contents of the memory will not be changed.

DMA Parity Error (A02)

A02 will set to indicate that a parity errory occurred during a data transfer to or from memory (Write, Read or Compare).

Lost Data (A03)

Indicates when set a DMA lost data condition.

Checkword Error (A04)

This bit indicates that the controller logic has detected an incorrect check-word in a data read from the disk during a Read Data, Compare Data or a Checkword Check operation.

Compare Error (A05)

This bit indicates that the data received from computer memory does not compare with data read from disk during a Compare operation.

If compare error occurs during Compare operation, but the Block Length is not terminated, the Controller stops the data transfer from memory at the end of the sector then the checkword check is determined and the Controller becomes Not Busy.

End of Medium (A08)

This error condition bit indicates that the controller tried to access a cylinder greater than 203 for single density CDD's or 406 for double density CDD's during a Read Data, Write Data, Compare Data and Checkword Check operation.

Controller Seek Error (A09)

This bit indicates that the controller found after reading the address field written on the disk, that the drive is not on the expected cylinder. After this error occurs, the CPU may read the True Cylinder Status (File "14+15") and compare it with the Cylinder Address Status (File "2+3").

Missing Index/Sector Pulse (A10)

This bit indicates that an index or sector pulse was not detected.

Wrong Sector Format (A11)

This bit indicates that a CRC error was detected in the address field, or that the sector format does not comply with the standard or that the sector format does not comply with the standard or that the controller searches a sector beyond the limits of 0 through 28.

Wrong Device Transfer (A12)

This bit indicates that a hardware error (no clock, no ready, device fault) occurred during data transfer to the disk or from the disk.

Bus Relinquished (A13)

This bit indicates that bus control was relinquished by the Controller in response to a forced request by the alternate Controller.

Block Length Status (File "8+9")

This status indicates how many data words remained to be transferred when the data transfer was terminated. A successful data transfer will have a Block Length Status of $FFFF_{16}$ (Write Data, Compare Data) or $FFFE_{16}$ (Read Data, Checkword Check) at EOP.

If the data transfer was not successful, the Block Length Status is:

a. B.L.-1 for Read Data and Checkword Check operations.
b. B.L.-3 for Write Data and Compare Data operations.

Checkword Status (File "10+11")

The Checkword Status may be used to monitor the checkword data read from the disk on a previous Read Data or Checkword Check operation.

True Sector/Surface/Disk Status/Inverse Disk Status (File "12+13")

This status contains the actual sector/surface/disk address information as read by the controller from the address field of the sector.

NOTE: If the controller is in the Inverse Disk mode, the disk status bit will reflect the requested disk, although the actual (physical) disk status will be the inverse of that which is specified by the disk status bit.

True Cylinder Status (File "14+15")

This register contains the actual cylinder information as read by the controller from the address field of the sector.

Seek Complete Status

Figure 2-20 illustrates the A-register bit assignments.

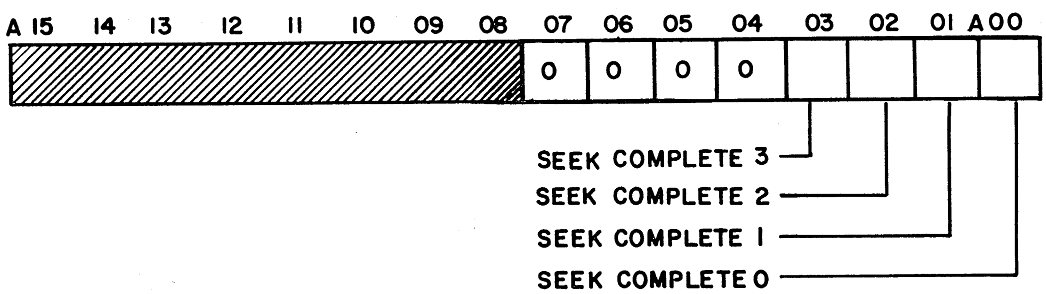


Figure 2-20. SEEK COMPLETE STATUS A-REGISTER BIT ASSIGNMENTS

These four bits when set are used to indicate that the corresponding unit has completed a seek operation (Seek Complete) or is unable to complete a seek operation properly (Seek Error). This status is available without the unit being selected. If a seek error occurred, bit A13 (Device Seek Error) in Dynamic Status will be set if the corresponding unit is selected. The Seek Complete Status command is rejected if the controller is busy. A reset bit indicates that the corresponding device is performing a seek operation, or that the corresponding device is after Director Function operation (except Write Address) or that the device is not On.

Uncrating

The Cartridge Disk Drive Controller (CDDC) printed circuit board is a 11 in. by 13.5 in. (279.4 mm by 342.9 mm) board shipped in a heavy-duty cardboard carton and is buffered from shock and impact damage by an industrial filler.

Inspection

Inspect the CDDC as follows:

1. Remove the CDDC printed circuit board from its shipping container.
2. Inspect for physical damage to the board and its components.

Power Requirements

The Cartridge Disk Drive Controller receives its +5 V dc from the power source. of the micro processor by connection to the backplane card slot of the CDDC. The CDDC may be connected to any AQ/DMA card slot.

Signal Cabling

The CDDC is supplied with a single 20-foot (6.1 meter) cable for connection from the device to the controller. Figure 3-1 shows the cable connection to the computer backplane.

CAUTION

Insure power is OFF before inserting or removing the Cartridge Disk Drive Controller or the external cable from the backplane to the Disk.

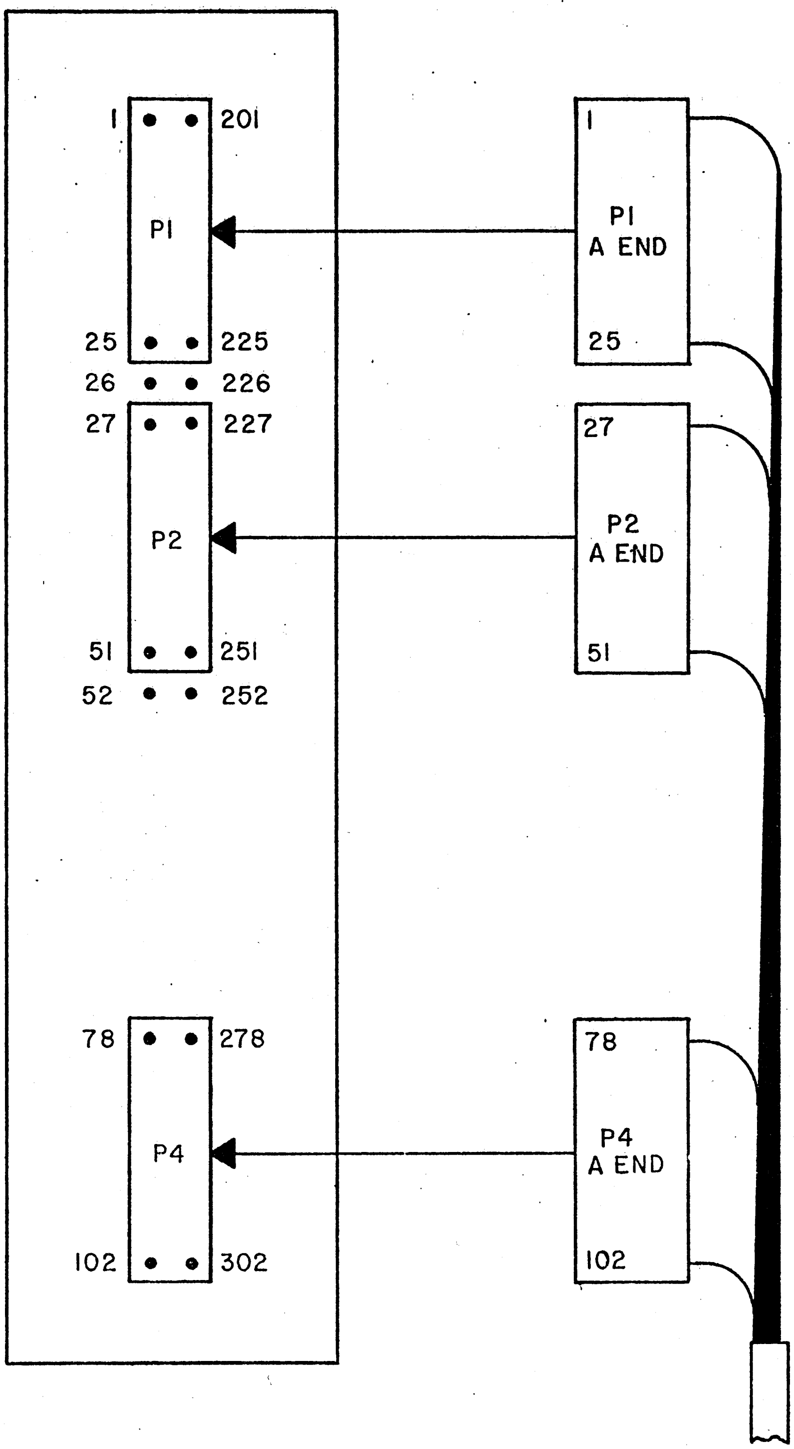


Figure 3-1. Cable Connection to the Computer Backplane

Operation

Issue the type of operation to be performed:

A. Write Data

B. Read Data

C. Compare Data

D. Any other Disk operations (Checkword Check, Write Address).

Status Checks

A. Check the Dynamic Status for Busy, EOP and Alarm.

B. If the Alarm bit is set, branch to an error recovery routine.

C. If the Alarm bit is not set, the operation was successfully completed.

Overlap - Seek Operation

A. Bus Connect.

B. Interrupt Request

C. Unit Select

D. Seek to Device

E. Repeat steps A,B,C and D for the other CDD units.

F. Seek Complete Status

G. Wait for Seek Change.

H. When Seek Complete is obtained issue a Load Disk Address and continue as for single disk operation, using each disk in its turn.

RECOMMENDED OPERATING PROCEDURE

The basic operations which the controller performs are Write Data, Read Data and Compare Data. The other disk operations are preliminary parts of the basic operation. The Checkword Check and Write Address functions are primarily maintenance operations.

The following programming sequence is a suggestion only and may be used as a general guide, if desired.

Single CDD Operation

Bus Connect - Connect the CDD to the I/O bus.

Interrupt Request - Select EOP and/or Alarm Interrupts if desired.

Unit Select - Select the unit.

Seek to Device - Select the starting cylinder address for subsequent operation.

Wait for on Cylinder - Read Dynamic Status and wait for EOP and On Cylinder bits set.

Memory Bank Select - Select the initial Memory Bank address.

Block Length - Load the length of the data block.

First Word Address - Load the First Word Address of the data block to be transferred.

MAINTENANCE SWITCHES

On/Off Line Switch Operation

"On Line" position enables normal controller operation.

"Off Line" position removes the controller from the Controller - CPU Bus and places the controller in a Maintenance Mode. The type of operation performed is now a function of the positions of the Maintenance Switches.

Maintenance Switches Operation

These are two switches, valid in maintenance mode. The operation initiated on the first disk which is ready, by the maintenance switches, conforms to the following table:

TABLE 3-1. MAINTENANCE SWITCH OPERATION

MS 2	MS 1	OPERATION
Off	Off	Seek Cylinder 5
Off	On	Seek Cylinder 73
On	Off	Seek Cylinder 10
On	On	Seek Cylinder 146

Once in the maintenance mode of operation, to change the Maintenance Switches to its other position requires that the On/Off Line Switch first to be placed back in its "On Line" position and then flipping off the maintenance switch.

Note: a) Maintenance Switches MS3 and MS4 are not used.
b) Before the maintenance seek operation, the controller performs RTZS function.

JUMPER SELECTIONS

Autoload Enable Jumper

This jumper when inserted allows the CDD Controller to perform autoload operations. When this jumper is removed, the controller is disabled from performing autoload operations.

Single/Dual Bus Access Jumper

A single jumper when inserted indicates dual computer access to the disk I/O bus. For single CPU operation, this jumper should not be inserted.

Protect On/Off Jumpers

Four jumpers, one per CDD unit. The jumper when inserted allows only instructions from the protected area of computer storage to access the disk drive selected.

Equipment Number Jumpers

These four jumpers can be set to represent any digit, 0-15. They are used to assign an equipment number to the controller/drive. Any instruction sent by the computer must be accompanied by an equipment number (bits 7-10 of Q) that matches the jumper setting. The jumper is inserted if the equvalent Q-bit in the equipment number is 1. Q7 is the least significant bit.

Track Density Selection Jumpers

These four jumpers, one per CDD, indicate the type of CDD connected, 100 tracks per inch (TPI) or 200 TPI.

Simultaneous Bus Determine Jumper

This jumper determines which controller will gain control of the bus in the case of simultaneous bus requests from both processors. Control will go to the one which has the jumper inserted. When using two CPU's, one and only one, CDDC should have the jumper inserted.

Jumper Mode

This jumper must always be removed.

Table 3-2. LEGAL JUMPER COMBINATION SETTINGS

Jumper Name	Function	Inserted	Removed
Q07→Q10	Determine Equipment Code	Logic 1	Logic 0
ALD	Autoload Enable	Enable	Disable
SB	Single/Dual Bus Access	Dual	Single
UPO	Unit protect for unit 0	Unit Protected	Unit Unprotected
UP1	Unit Protect for unit 1	Unit Protected	Unit Unprotected
UP2	Unit Protect for unit 2	Unit Protected	Unit Unprotected
UP3	Unit Protect for unit 3	Unit Protected	Unit Unprotected
SD0	Track Density Selection for unit 0	Single (100 TPI)	Dual (200 TPI)
SD1	Track Density Selection for unit 1	Single (100 TPI)	Dual (200 TPI)
SD2	Track Density Selection for unit 2	Single (100 TPI)	Dual (200 TPI)
SD3	Track Density Selection for unit 3	Single (100 TPI)	Dual (200 TPI)
BP	Determine bus usage in case simultaneous bus requests.	This CPU	Alternate CPU
JM	Must always be removed	———	———

NOTE: For selection of equipment codes the jumper selection for Q07-Q10 must match Q07-Q10 from the CPU via A/Q.

Table 3-3. ON/OFF LINE SWITCH

Switch Name	Function	ON	OFF
ON/OFF Line	Selects ON LINE OR Maintenance Operations	Normal Operation	Maintenance Operation

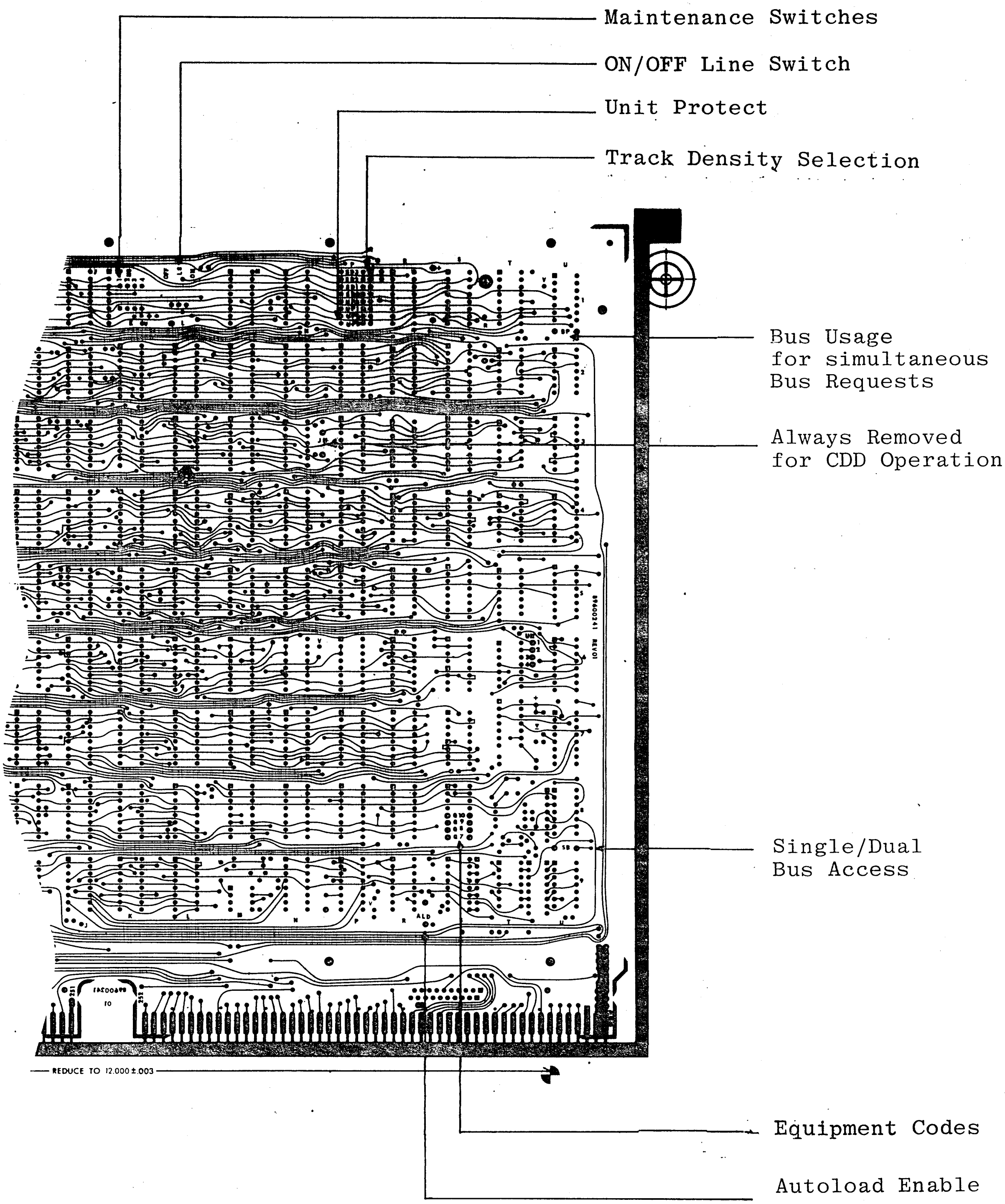


Figure 3-2. Jumper Locations

THEORY OF OPERATION

Introduction

This section presents general and detailed functional descriptions of the equipment using such aids as overall block diagrams and timing diagrams. Descriptions are keyed to the detailed logic diagram and create a basis for understanding the detailed description of the specific circuits in that section.

NOTE

It is assumed that the reader is familiar with the Control Data equipment and with the programming characteristics of this Computer.

The basic configurations are as shown in figures 4-1 and 4-2, and the overall block diagram in figure 4-3.

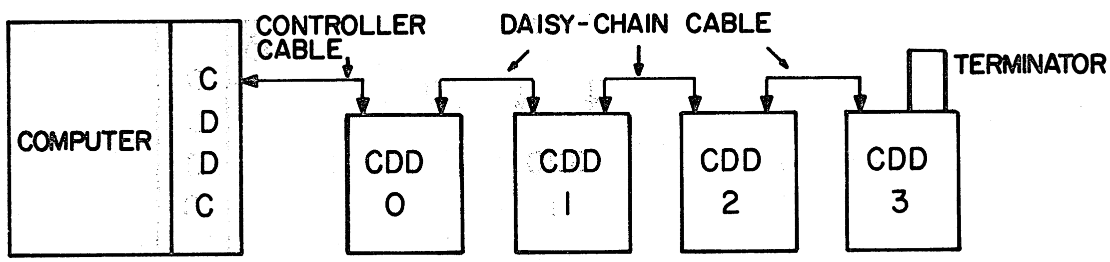


Figure 4-1. Single Computer Access

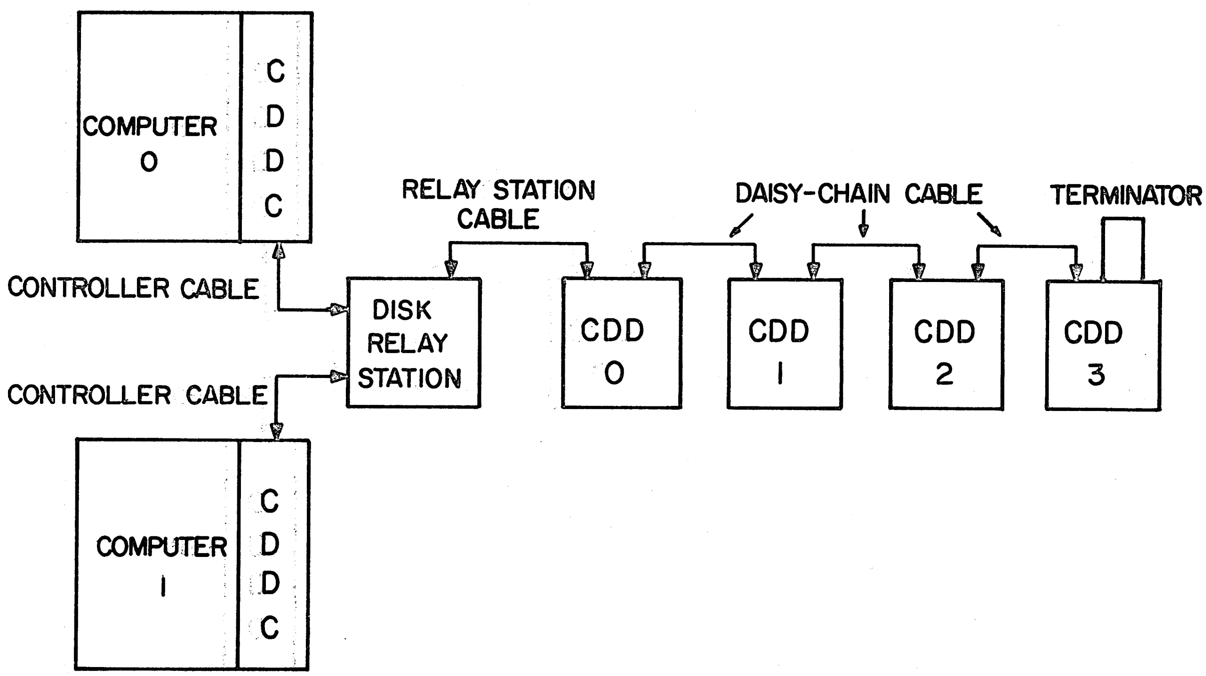


Figure 4-2. Dual Computer Access

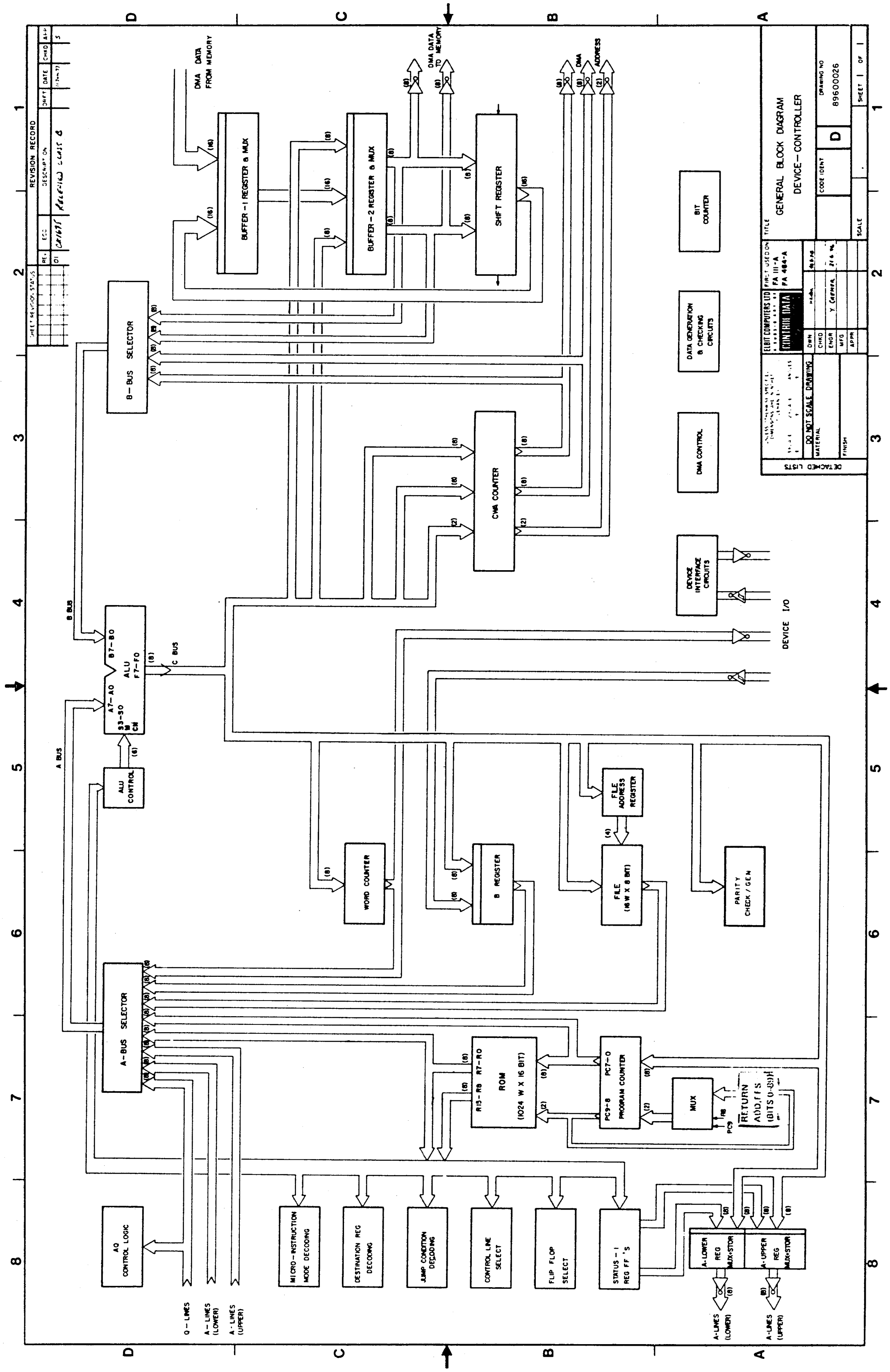


Figure 4-3. Block Diagram

The CDC Cartridge Disk Drive Controller contains the logic that interprets the CYBER 18 CPU function codes, controls the CDD operation, assembles, disassembles the 16-bit words between the CPU and the CDD, and provides the CDD status information to the CPU. Communication between the Controller and the CPU is via the A/Q channel for status, control information and test, and via the DMA channel for data transfer.

The CDDC uses the concept of micro-programming. It consists of TTL logic components mounted on one CYBER 18 printed circuit board; the board occupies one (Dual Port) AQ/DMA slot in the CYBER 18 mainframe.

The CDDC has these additional characteristics:

1) Provides Autoload capability to the CYBER 18 processor from any one of the CDD's.

2) Provides maintenance capabilities, off-line, to any one of the CDDs.

3) Allows dual CPU access to the CDD's.

4) The CDDC handles any combination of BR704-A & -B CDDs, all operating at 2400 RPM.

5) Provides interface control for up to four CDD's connected in daisy chain fashion. A single cable will connect the controller with the first CDD, and each CDD will have two identical interconnection plugs to enable the daisy chain configurations. Figures 4-1 and 4-2 show possible CDDC/CDD configurations.

Controller/CDD Interface Signals

The following is a list and description of each of the controller CDD interface signals:

Device Input Signal Lines

The Input lines carry the following signals:

CYLINDER ADDRESS STROBE (CA STROBE)

This signal gates positioning information into the CDD. The positioning information is contained on the TA bit lines and is equal to the desired track address. The controller must receive an On Cylinder signal before sending a TA Strobe.

CYLINDER ADDRESS BITS (TA Bits)

These signals are carried by nine lines which transmit the desired track address.

RTZS (Return to Zero Seek)

This signal initiates positioning motion to cylinder 000 on the leading edge of the RTZS pulse (typically 1 μsec). The RTZS pulse may be repeated with the following limitations:

a) An RTZS pulse may be sent whenever On Cylinder is present from the CDD.

b) An RTZS pulse may be sent without On Cylinder present if at least 300 μsec has elapsed since the last RTZS pulse or TA Strobe pulse.

NOTE

The RTZS function should be issued to clear the seek error condition.

HEAD SELECT

One line carries the signal that selects one of the two recording heads (two lines are utilized for four heads when using the fixed disk option). The signals represent the binary address of the desired head and must be held constant during a read or write operation.

WRITE GATE

This signal enables the write current in the write head coil.

ERASE GATE

This signal enables the erase current in the erase head coil.

Head Select 2^1 (DISK)	Head Select 2^0 (SURFACE)	
0	0	Selects cartridge top head
0	1	Selects cartridge bottom head
1	0	Selects fixed disk top head
1	1	Selects fixed disk bottom head

WRITE DATA/CLOCK

One line carries the double frequency clock and data information signals to the CDD.

READ GATE

This signal enables read data and clock information.

UNIT SELECT (Daisy Chain Option Only)

Four lines (one per unit) are used to select the required unit. The signals must remain "on" during all communication with the unit except for monitoring of the seek-complete signal.

TERMINATOR POWER

+5 Vdc 630 mA (typical) terminator power for the CDD transmission system is supplied by the CPU via the controller.

TERMINATOR MONITOR

This line is monitored by each unit to sense the loss of controller power as indicated by loss of terminator power. This line should be terminated to +5 Vdc through 150 ohms at the controller end and 100 ohms at the drive end. In the event of controller power loss the Unit Select is disabled. The unit will not respond to any commands until power is restored.

TRACK OFFSET

Only during a read operation can a logic 1 on the line cause the heads to undergo a 500 millisecond slow period. In this time the head displacement is zero controlled, directed radially inward and outward and having a nominal amplitude of 1000 micro-inches.

Output Device Signal Lines

The output lines carry the following signals:

ON CYLINDER

A logic 1 on this line indicates that the selected unit has completed a seek operation and that the heads are positioned on the new cylinder address. The selected unit is now ready to seek, read, or write, provided that a fault condition is not present. A logic 0 on this line indicates that a seek operation has not yet been successfully completed.

READ DATA

This line carries Data pulses.

READ CLOCK

Read Clock signals are carried on this line.

INDEX

This signal is the index pulse from the cartridge which appears once in every revolution.

SECTOR

This signal is the sector pulse from the cartridge which appears at the beginning of each of the twenty-nine sectors.

SEEK ERROR

This signal indicates that the heads have moved to an illegal address or that a seek was not completed within 200 msec. An RTZS command sent to the unit indicating a seek error, will clear the seek error condition, return the heads to cylinder zero, and enable an On Cylinder signal to be sent to the controller.

DISK WRITE PROTECTED

This signal indicates that the CDD is Write protected. If the "Write Protect" switch is set in the Disk Drive, writing (data and address) onto the Disk is disabled.

FAULT

This signal indicates that the CDD has one or more of these fault conditions:

a) Multiple head selection.

b) Read and Write gate enabled at same time.

c) Read and Erase gate enabled at same time.

d) Erase current and no Write gate.

e) Write current and no Erase gate.

f) Read, Write or Erase gates and no On Cylinder.

g) Low voltages present (below specified values).

h) Fixed-disk heads are selected with no fixed-disk option installed.

i) Emergency retract condition.

UNIT READY

This signal indicates that the CDD is in a state of readiness, i.e., cartridge in, disks up to speed and heads loaded.

SEEK COMPLETE OR SEEK ERROR
(Daisy-chain option only)

Four lines carry signals to indicate that the corresponding unit has completed a seek (Seek Complete) or is unable to complete a seek (Seek Error). This is a signal transmitted with or without the unit being selected. The seek complete is a static "1" which is cleared by a selected read gate or another seek command. A Seek Error will cause the Seek Complete/Seek Error line to become true. Only a RTZS can recalibrate the device and clear the error condition.

MICROPROGRAMMING CONCEPT

Initiation

Power on Master Clear or Clear Controller resets the program counter. Upon expiration of the MC or CC pulse, micro-code execution will commence from ROM location zero. These conditions will reset the PC:

1) Master Clear (Power On)
2) Clear Controller
3) Force Bus Release

The micros determine the reasons for the PC reset so that appropriate action may be taken. At first, the ALT FORCE line is sampled. If it is active, a jump is made to the bus relinquished routine which sets the proper status bit in the alarm word to inform the CPU of the bus relinquish condition and to set the interrupt response if the alarm interrupt request is active.

Next, the ROM Execute F F is sampled. This F F is used to inform the micros that an A/Q command was received from the micro processor. The ROM Execute F F being active informs the program that a Clear Controller command has been received. The micro will reset the appropriate status and will issue a reply.

If neither ROM Execute or Bus Force are active, the reason for the PC reset is assumed to be Master Clear.

For all these PC reset conditions, the program will flow through an initialization routine which will set the proper operating F F's and status and will then flow into the waiting loop.

The Waiting Loop

The controller initiates all of its operations with the exception of Clear Controller and Dynamic Status Request from the waiting loop. This loop continuously samples the following jump conditions:

1) A/Q Execute F F - This F F will become active whenever an A/Q command with Q4=0, and with the proper equipment code is received.

2) Autoload - This line will be activated when the micro processor switch is pushed.

3) On/Off line switch - Whenever the off-line maintenance switch is pushed in the off-line position, this line will go low (active).

4) Alternate Bus Request - When the controller is on Bus, it will cause an interrupt response if the alternate bus interrupt request is active.

Whenever any one of the above conditions is active, an exit will be made from the waiting loop and the required action will be performed. All actions are terminated by a return to the waiting loop.

A/Q Execute

The Q line bits 0-4 (function code) together with the WRITE signal occupy one input to the A bus selector. When the A/Q execute F F is detected as active by the waiting loop routine, the Q input to the A bus selector is sampled twice to prevent noise on the A/Q channel from causing an unwanted operation. If the two samples are not equal, the controller rejects the operation. Then it is masked and loaded directly into the PC. This preload causes a 32 way main program branch. Each of the 32 branch locations contain the starting address of the routine which performs the function whose code is found in Q00-Q04 and the Write signal. Not all of the 32 function codes are valid. The branch location of illegal codes contains a jump to the reject routine.

As an example of the preload, assume that the First Word Address function (Q=602) is received. Since this function is initiated by an output instruction, the WRITE signal will be active. The Q input to the A bus selector will look like figure 4-4.

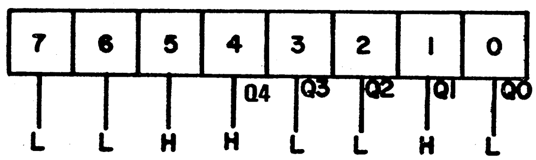


Figure 4-4. Q-Input to A Bus

Bits 06 and 07 are always low. Bit 05 will be high because the WRITE signal is active; bit 4 will be made high by a program mask operation; bits 03, 02, 00 are low and bit 01 is high. When this code (32_{16}) is loaded into the PC, a branch will be made to ROM location 32_{16}. ROM location 32_{16} contains a branch instruction to the start of the First Word Address routine. Bits 08, 09 of the PC are forced to zero by the hardware before the preload operation.

The routines for executing each one of the A/Q functions can be divided into two categories: those which cause the controller to go busy and those which do not. The former can be subdivided into Controller/CDD preparation and Director function operation.

Non-Busy Routines

Routines which do not cause the controller to go busy (such as First Word Address) are checked for property to determine whether they will be accepted or rejected. The conditions for reply or reject for each command are given in the Engineering Specification for the Cyber 18 Cartridge Disk Drive Controller.

Once a reply or reject is issued, a jump back to the waiting loop is made. The following is a description of the non busy functions:

First Word Address

The data received from the CPU is moved from the A low and A up input to A Bus Selector via the ALU to the CWA_{up} and CWA_{L} (CWA low) registers. These registers provide 16 bits of the address during DMA transfer operations. At the completion of the transfer, the CWA register is incremented. Overflow from CWA will increment the Bank register.

Bank Select

Bits 06 and 07 of the A up are transferred into the Bank register. This register provides the upper two bits of the DMA address.

Load File Address

The lower 8 bits of the A (Al) are transferred to the B Register. When file status is requested, the contents of the B Register are transferred to the File Address register.

Block Length

The data received on the A lines is transferred to file address 8 and 9. File address 8 will contain the lower 8 bits and address 9 will contain the upper. During Data transfers file address 8 is decremented. If this also yields a Borrow Out, it is an indication that the entire block length has reached zero and the transfer is to be terminated.

Interrupt Request

All bits A7, A6, A5 and A3 are monitored. If bit A7 is one, it indicates that a clear interrupt command is issued, so the controller resets the interrupt response and A1 is transferred with "shifting left" into File register 4. If bit 07 is zero, the controller executes ORing of the "A_{LOW} shifting left" with the contents of File 4 and inserts it into File 4. Figure 4-5 demonstrates the Interrupt Request register: (File 4).

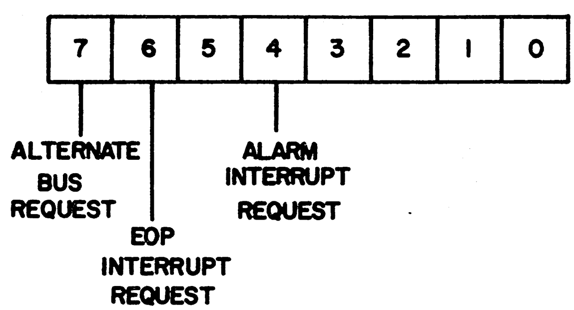


Figure 4-5. Interrupt Request Register

If Alarm Interrupt Request is active or Alternate Bus Request is active, the appropriate status is tested and if it is active, the interrupt response is activated.

Load Disk Address

The data received on the A lines is transferred to file 2 and 3. This function is used for reloading the cylinder address register after performing overlap-seek operations.

A-Out Status

This routine simply issues a reply, sending the content of the controller A-out register to the CPU.

Current Word Status

The contents of the CWA register is transferred to the A-Out register allowing the CPU to read the Current Word Status.

Current Bank Status

The two bits of the Bank register are decoded by micro and a 0, 40_{16}, 80_{16}, CO_{16} will be placed in the A out upper according to the result of the decode.

File Status

The contents of the B register are loaded into the file address register. The contents of the file are loaded into the A out L register. The B register is then incremented by one and again loaded into the file address. The file contents are then transferred to the A out up register.

Seek Complete Status

The controller will sample the 4 seek complete lines of the CDD's and place it in the bit position corresponding to that unit.

Busy Routines

For functions which cause the controller to go busy, a check is also made as to the priority of the command. If all conditions for acceptance are present, a reply will be issued and the busy F F will remain set for the duration of the operation.

Completion of the operation will cause a branch to a terminated busy routine. This routine sets the proper initial conditions which might have been changed by the previous routine, checks whenever an EOP or Alarm Interrupt is to be generated, resets the busy F F, sets EOP status, and returns to the Waiting Loop.

Preparation Routines

The following two commands, Bus Connect and Unit Select, are necessary for all CDD operations.

Bus Connect

Normal Request (A05 = 0; A07 = 1)
The CDDC will first check bus usage. If the bus is in use by the alternate controller, the CDDC will raise a flag (Bus request) to the alternate controller to notify the alternate that it requires the bus. During this time, the CDDC requiring the bus will be busy. When the bus does become available, the CDDC will gain control and will notify its CPU by setting the On Bus status and by generating EOP status and EOP interrupt (providing EOP interrupt was selected).

Force Release (A05 = 1; A07 =1)

The CDDC which requires the bus will send a Bus Force signal to the alternate controller. This signal has the same effect on the alternate as a Master Clear and will cause the alternate to release the bus immediately. In addition to the Bus Force signal (Master Clear), the CDDC will send a Forced Release Status signal to the alternate.

This signal will allow the alternate to differentiate a force bus signal from a true Master Clear signal, and thus, notify the alternate CPU that a forced bus release took place. Having forced the alternate off the bus, the CDDC will gain bus control and will notify the CPU of this condition in the same way as for a normal request.

Once bus control has been established, the CDDC which is "On Bus" may be obliged to relinquish the bus in response to a Force Signal from the alternate. Relinquishing of the bus causes the Alarm Status Bit and Bus Relinquish Status (bit 14 of the alarm status word) to become active. An Alarm Interrupt will also be generated provided that Alarm Interrupt was selected.

A Force Release signal from the alternate has the same effect on the CDDC as a Master Clear with the exception that Interrupt Requests are not affected by this signal.

UNIT SELECT Routine

This routine is used to select one of the CDD's, check the protect jumper of this unit and update the controller protected F F. Also it checks and updates the density status of this unit and the Inverse mode register (File 12).

SEEK TO DEVICE Routine

This routine strobes the cylinder address from the A lines to the W.C. register in the controller and initiates the head positioning motion in the CDD.

In addition, it fills the cylinder address register in the controller. The controller goes busy just long enough to initiate the seek command and then goes not busy, thus allowing overlapseek operations on the four CDD's.

WAIT FOR SEEK CHANGE Routine

This routine will transfer the A line bits 0 to 3 which specify the initial unit seek complete status to the controller.

The controller will sample the seek-complete status of each of the four units and the result of this sampling will then be compared with the unit seek-complete status originally received from the CPU via the A register. The sample and compare operation will continue until the original seek-complete status and the actual (sampled) seek-complete status are not equal. This indicates that one or more of the units which were previously not seek-completed have become seek-completed (or vice-versa). EOP status and EOP interrupt (if requested) will be generated when a change in the seek-complete status occurs.

Director Functions

Once a bus connect and unit select are made, all operations with the CDD's (except Seek to Device) are initiated via a Director Function Command.

When the Q function code is decoded as 31_{16}, a branch is made to the Director Function routine. This routine checks that the controller is on bus, the unit is ready and if any one of these conditions is not true, the command is rejected. Then A LINE bit 5 is checked and if set a jump to RTZS Routine is made. If all the conditions are true and A bit 5 is 0 a reply will be issued and the busy F F will be set. (See figure 4-6.)

Bits 14 and 15 are checked for updating the disk and surface heads (in the disk F F setting, consideration will be taken on the inverse bit mode) and the A up is loaded into File 1 (sector, disk surface register). Then On Cylinder and Seek Error conditions are checked and if they are wrong, alarm is set and the operation is terminated.

The 4-bit Director Function Field A00-A03 is decoded in the same manner as in the Q Function Code. This field is sampled twice for prevention of noise, then masked and loaded directly into the PC. This causes an 8-way micro program branch only, because A03 is always 1.

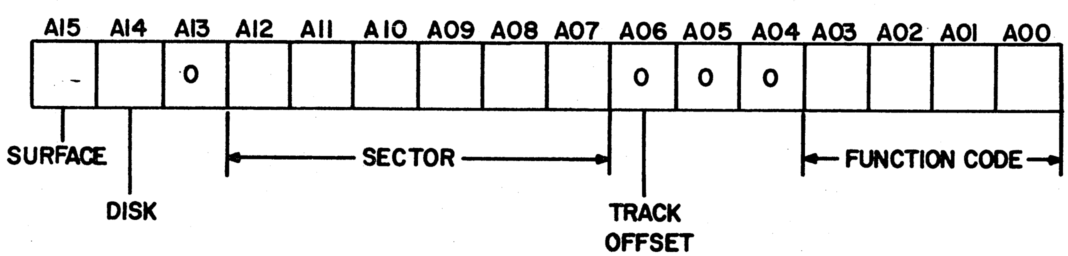


Figure 4-6. A Register Bits For Director Functions

WRITE ADDRESS Routine (See figure 4-7)

This routine causes the Controller to write the address tags of all the sectors in the presently available track specified by the contents of the cylinder address register (File 2-3).

After the Director Function is decoded as a Write Address, the Controller waits for the leading edge of the index mark and then the writing of the address field in the first sector is begun. Each sector is divided into fields as shown in the figure on the next page.

After the end of the sector, the routine calls the advance subroutine which computes the next sector number and checks if the last sector was operated on.

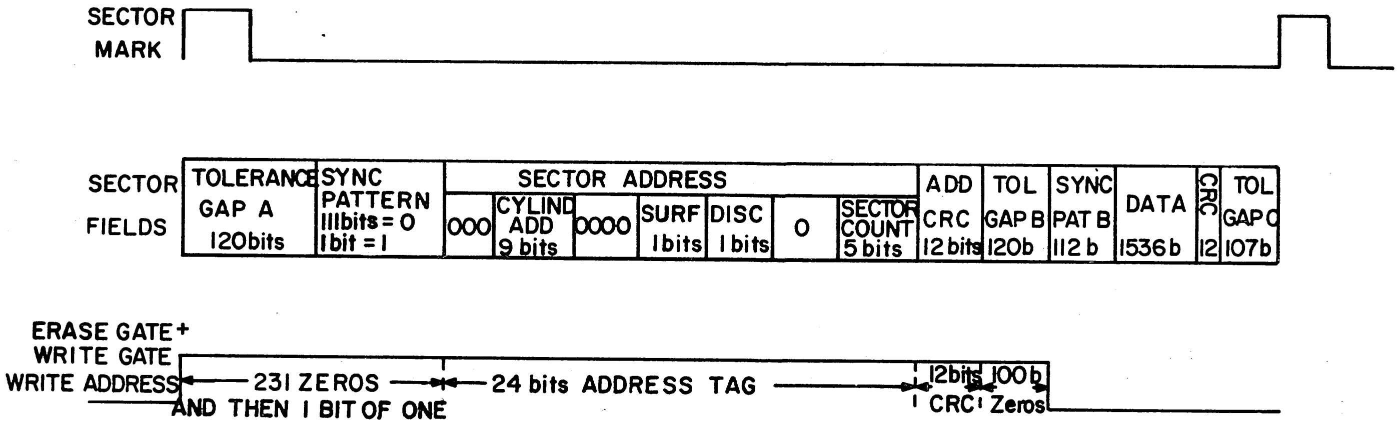


Figure 4-7. Write Address Routine

The address tags are written sequentially from 0 to $1C_{16}$. Detection of abnormal conditions (Not Ready, Not On Cylinder, Device Seek Error, Missing Index/Sector Pulse, or Disk Write Protected) by the Controller causes the operation to cease and the corresponding status bits and the alarm bit to be set.

<u>Sense Verify</u> (See figure 4-8)

This routine causes the Controller to read the address of the sector currently under the read head. It fills File Register 12 and 13 with the results.

Upon detection of Sense Verify function, the sense F F is set and the Controller is entered to the Search sector subroutine. This subroutine reads the address tag, compares the expected cylinder to the true cylinder and searches the desired sector number. Exit will be made from this subroutine immediately after reading the first sector address and comparing it to the expected cylinder if the sense F F is set.

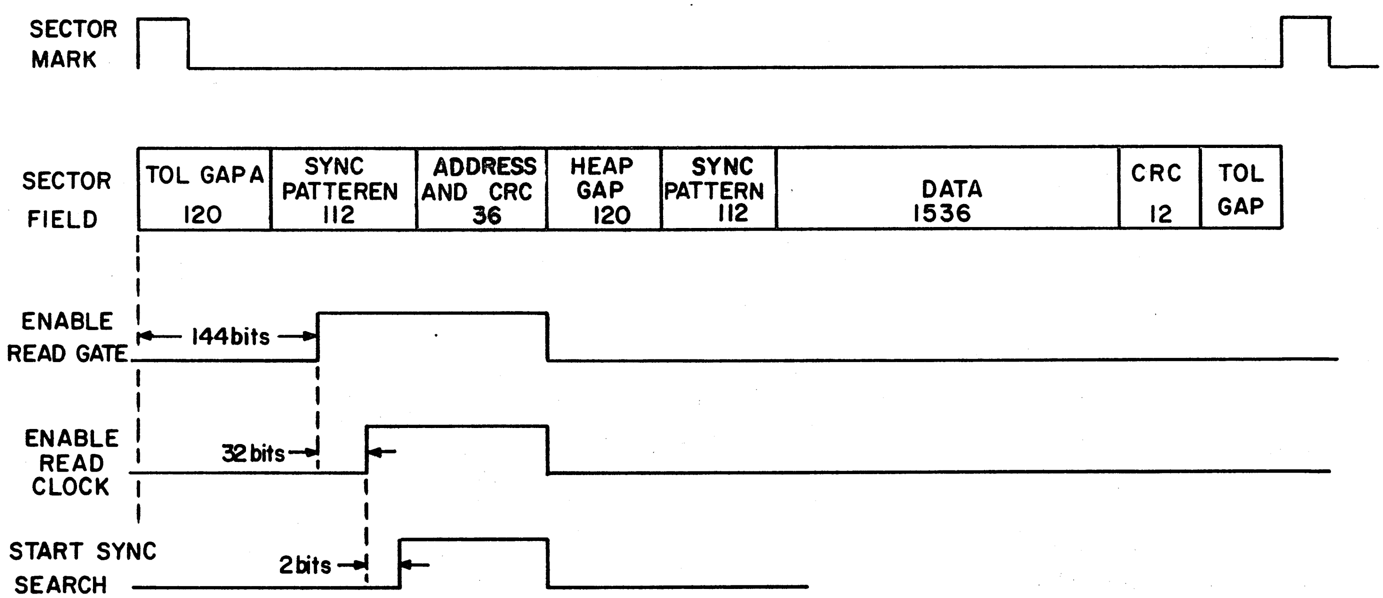


Figure 4-8. Sense Verify Routine

READ DATA

The Read Data function directs the Controller to transfer data from the disk file memory to computer storage. First data is read from the disk starting at the location that is specified by the preceding seek and the A up of the Read Data command. Then it is transferred to the memory starting at the First Word Address until the number of words specified in the Block Length has been transferred. Figure 4-9 describes activation of the read gate during this operation.

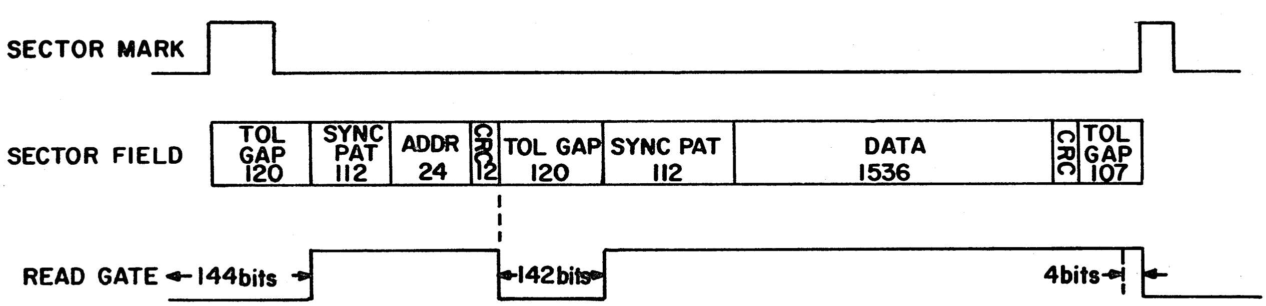


Figure 4-9. Read Data Function

Upon receipt of the Read Data function, calling of the search sector subroutine is made. This subroutine finds the desired sector and after synchronizing to the sync pattern of the data field, data transfer will begin.

When the Bit counter indicates that a 16 bit word has been assembled in the shifter, the word is transferred to Buffer 1. If Buffer 2 is empty, the word is immediately transferred to Buffer 2 and the DMA-REQ FF is set. Upon receipt of the storage REQ-ACCEPT signal, the data is transferred from Buffer 2 to the memory location as specified by the Current Word Address.

If Buffer 2 already contains a word the new word will remain in Buffer 1 until Buffer 2 is emptied and the controller will raise the priority signal to the memory. During the time that this word remains in either buffer, serial data is continually read from the disk to the shifter. If another word will come from the DISK and the two buffers are still full, lost data occurs and causes the operation to cease.

The serial parallel assembly and transfer to the DMA continues until the WC is decremented to zero, indicating the end of the Data Field of this sector. After that the 12 bits of the CRC field are read and the CRC circuit is inspected for a non-zero content which indicates a checkword error.

Thereafter, if the Block Length is not empty, the routine calls the advance subroutine which takes care of the following operation. If data transfer to the computer stops within a sector, the controller continues reading the data until the end of the sector and determines if the checkword is correct. If the data transfer extends beyond the last sector of the "top" surface, the transfer continues from the first sector of the "bottom" surface. If data transfer extends beyond the last sector in a cylinder, the advance subroutine moves the cylinder positions to the next cylinder and continues the transfer there. If transfer is attempted beyond the last cylinder in a disk, an End of Medium error will occur during the data transfer.

Several abnormal conditions can develop during this operation. Detection of these conditions by the controller cause the operation to end. The abnormal conditions are:

1. Unit becomes Not Ready
2. Unit becomes Not On Cylinder
3. Device Seek Error
4. Missing Index/Sector Pulse
5. Controller Seek Error
6. Wrong Sector Format
7. Wrong Device Transfer
8. Lost Data
9. DMA Address Error
10. DMA Protect Fault
11. DMA Parity Error
12. Checkword Error
13. End of Medium

Detection of any of the abnormal conditions causes the corresponding status bit and the Alarm bit to be set.

In return from the advance subroutine, the routine again calls to the search sector subroutine until the specified block length has been transferred from the disk to the Memory.

WRITE DATA

The Write Data function directs the controller to transfer data from the computer memory to the CDDC via the DMA channel. Data is read from the computer memory starting at the first word address and transferred to the disk from the location specified by the preceding seek and A up of the Write Data command. The transfer continues until the number of words specified in the block length have been transferred. Figure 4-10 describes the activation of the Erase Gate + Write Gate and Read Gate during this operation.

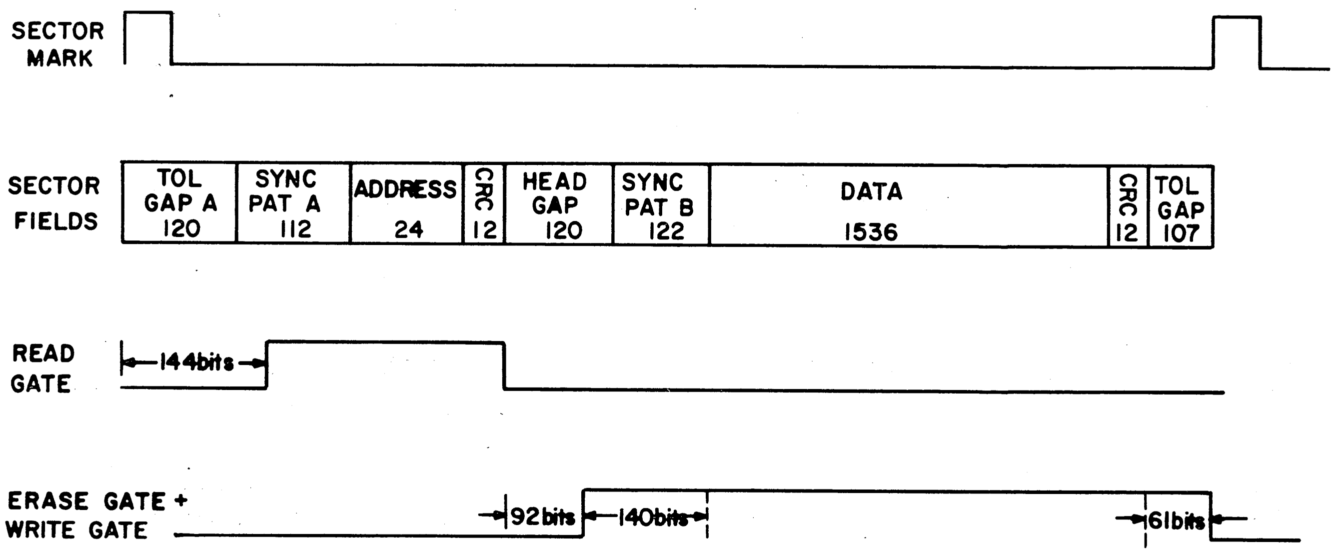


Figure 4-10. Write Data Function

This routine uses the same two subroutines as read data: Search Sector Subroutine and Advance Subroutine.

First the controller calls the Search Sector Subroutine. The first step of this subroutine is to decrement three words from the B lower register. This gives the Micros an indication when the last three words are transferred and to stop the automatic Double Buffer transfer. This ensures that no more words than are needed are stacked in the Double Buffer. Then the controller searches the desired sector.

After the controller finds the desired sector it counts 92 bits and begins to write 139 zeroes and then 1 one. After the one is written it begins to write the data. When the controller is two words before writing the last 1 in the sync pattern the micros fill Buffer with 0001_{16}. Then a DMA REQ is sent to the CPU and a word is transferred from the memory into Buffer 1.

The transfer of a word from Buffer 2 to the shifter causes the transfer of a word from Buffer 1 to Buffer 2 and the generation of a DMA REQ. For Write, Read and Compare, when a word is transferred from Buffer 1 to Buffer 2 the hardware always generates a DMA REQ. signal. If the Double Buffer contains one or no word, the controller sends a priority signal to the memory. If the current word was shifted and no word was in the Double Buffer lost data will occur.

Serial data being transferred to the disk is first inserted into the CRC chip. After the last word in the sector is transferred, the 12 bits that were created in the CRC chip are transferred to the disk.

If the data transfer ends within a sector, the controller fills the remainder of the sector with zeroes and then writes the checkword. If the buffer length is not empty the advance subroutine computes the next operation and the search sector subroutine is called again.

The advance data transfer is as follows: If the data transfer extends beyond the last sector of the "top" surface, the controller will automatically continue the transfer on the first sector of the bottom surface of the same cylinder. If the data transfer extends beyond the last sector in a cylinder, the controller will move the cylinder positioner to the next cylinder and continue the transfer there. If a transfer is attempted beyond the last cylinder in a disk, an End of Medium error will occur. No switching from a fixed to removable disk, or vice versa, occurs.

Several abnormal conditions can develop during this operation. Detection of these abnormal conditions by the controller causes the operation to cease.

These abnormal conditions are:

1. Device Seek Error
2. Unit becomes Not Ready
3. Unit becomes Not On Cylinder
4. Missing Index/Sector Pulse
5. Controller Seek Error
6. Wrong Sector Format
7. Wrong Device Transfer
8. Lost Data
9. DMA Address Error
10. DMA Parity Error
11. End of Medium
12. The Disk is Write Protected

Detection of any of these abnormal conditions causes the corresponding status bit and the alarm bit to be set.

Compare Data

The Compare function causes the disk controller to internally compare data read via the DMA from the memory with data read from the disk. The number of words to be compared is specified by the preceding Load Block Length function. The starting location on the disk is that specified by the A up lines of the Compare data command and the preceding SEEK function. As in the Read and Write functions, the heads will automatically be advanced until the number of words specified by the Buffer Length have been compared.

With respect to the transfer of serial data from the disk, the Compare function operates identically with the Read function. With respect to the transfer of parallel data from the memory, the Compare function operates identically with the Write function. The actual data processing is done serially with a bit-by-bit comparison between the data read from the disk and the data read from the memory and converted to serial form by the Shifter. Upon detection of the first mismatch, the Compare Error status is set. However, the comparison operation continues to the end of the current sector and the checkword is checked.

Checkword - Check

The checkword check function directs the controller to read the data from the disk into the checkword logic to be checked until the number of words specified in the Block Length have been transferred. (The controller continues reading the data until the end of the sector.) The operation is the same as for a Read Data command except that no data is transferred to or from the computer memory.

Return to Zero Seek (RTZS)

This command recalibrates the selected drive and causes the heads of the selected disk unit to be positioned on cylinder zero. The RTZS function will clear the Drive Seek Error condition, and the Alarm bit in the Dynamic Status.

Autoload

Depressing the switch located on the front of the MP processor will cause the autoload jump condition to go low. When this jump condition is sensed in the waiting loop, the following will occur:

1. Connection of CDD Controller onto the device bus.
2. Selection of the first unit which is ready.
3. Recalibration (RTZS) of that unit.
4. The Reading of the twenty-nine sectors of the upper surface of track zero of the removable disk.

This data will be loaded into the computer memory low order bank, starting at location zero.

Several abnormal conditions can develop during this operation (see read data section for a list of these conditions). Detection of these conditions by the controller will cause the operation to end.

If the autoload switch is pushed while the controller is on-bus, the autoload command will be ignored. Therefore, Autoload must always be preceded by Master Clear. Autoload data transfers are made using full write cycles ignoring the DMA protect and parity faults.

Pressing the autoload pushbutton while the controller I/O pin 23 is shorted to ground will cause the autoload operation to be done in the inverse mode, i.e., the twenty-nine sectors of the upper surface of track zero of the Fixed Disk will be read.

Self Tests

The controller has four self tests for checking hardware via firmware. Self test 1 checks the internal controller data paths and ALU operations. The data received from the CPU is divided into the upper and lower portions called A up and A low and transferred via the ALU to the B register and BR2 low register. These registers feed the A and B sides of the ALU, respectively. The logical arithmetic operations specified by the self test 1 equation are performed on these two registers and the result is placed in the lower portion of the A-out register. The A low data is then transferred and incremented through all sixteen file registers and then through all of the controller registers, with the A-Out upper being the final destination of the data. The CPU can examine the self test 1 result contained in the A-out register by reading A-out status.

Self test 2 checks FF's and jump conditions. A clear controller command must be received prior to Self test 2 to insure that all the FF's are in the reset state. Every FF that is connected to a jump condition and which should be reset by a clear controller pulse is tested to check if it is in reset condition. Any active FF will cause the hex number DEAD to be placed in the A-out register and the program will return to the waiting loop.

After the reset condition test is completed, the FF's are set and tested for the set condition. The Shift register, the Double Buffer with its Control of data circuit, the First and all other jump conditions which can be activated by micro code are also tested both in their set and reset states. If all tested conditions are in the proper state, the program will write $ACED_{16}$ into the A-out register and return to the waiting loop.

Self test 3 initiates a DMA read request. The data read is placed into the A-out register when it is available to the CPU as status.

Self test 4 moves the data in the Ain low and the Ain up to the BF2 low and BF2 up registers respectively and then initiates a DMA write cycle. When the cycle is complete, control passes back to the waiting loop.

Off-Line Maintenance

All of the off-line maintenance operations are initiated by the detection of an active signal on the off-line maintenance jump condition during the waiting loop. An exit is made from the waiting loop to a maintenance initiation routine which will cause:

1) CDD Controller to be connected on the device bus.
2) Selection of the first unit which is ready.
3) Recalibration (RTZS) of that unit.
4) Performs this operation:

MS2	MS1	Operation
Off	Off	Seek Cylinder 5
Off	On	Seek Cylinder 73
On	Off	Seek Cylinder 10
On	On	Seek Cylinder 146

Once in the maintenance mode of operation, changing the Maintenance Switches to other positions requires that the On/Off Line Switch first be placed back in its "On Line" position and then flipping off the maintenance switches.

MICRO INSTRUCTION DESCRIPTION

Most of the control logic with the Controller is implemented by micro instructions contained with Programmable Read Only Memory (PROM). This design approach replaces the more conventional hard-wired random logic.

To understand the Controller's logic the reader must first understand how the micro-control section operates and then how to follow the logical program flow as shown in the flow charts.

The following description describes the micro instructions and their implementation. The micro-program flow charts are shown in Appendix A.

THE MICRO INSTRUCTION REPERTOIRE

The micro instruction set is divided into 4 groups:

1. Inter-Register instructions.
2. Load Constant instructions.
3. Control Line and FF instructions.
4. Jump instructions.

The 16 bit micro instruction word is denoted R00 through R15, where R00 is the least significant bit. Figure 4-11 is a summary of the various micro instruction group formats.

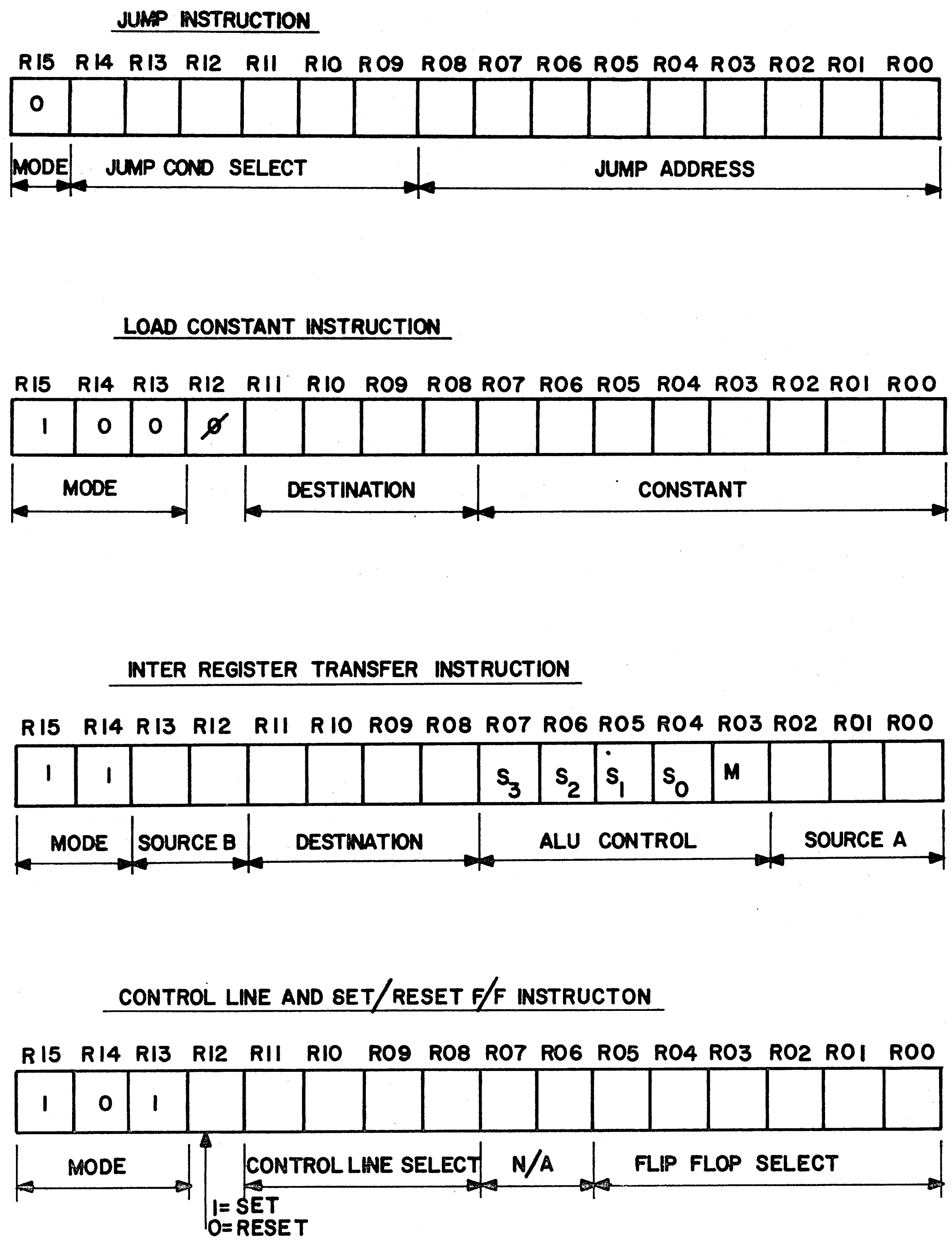


Figure 4-11. MICRO INSTRUCTION GROUPS

INTER-REGISTER MICRO INSTRUCTIONS

Inter-Register micro instructions are identified by R14=1 and R15=1. These instructions cause data from a combination of two sources to be sent through the ALU to a destination register. Various logic and arithmetic operations, selected by the ALU control lines, are performed on the data as it passes through the ALU. Figure 4-12 illustrates the instruction format.

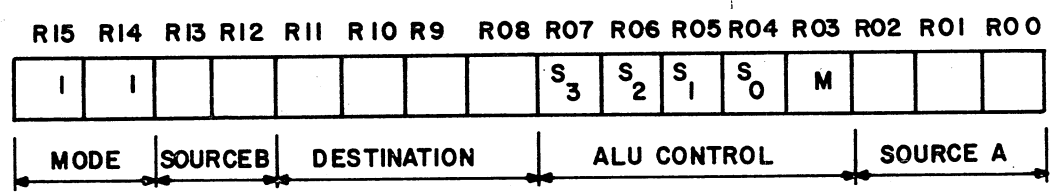


Figure 4-12. INTER-REGISTER MICRO INSTRUCTION FORMAT

The source A field bits R00, R01 and R02, select one of seven available source A registers. Table 4-1 provides the Source A codes.

The Source B field, bits R13 and R12, select one of four available Source B registers. Table 4-2 provides the Source B codes.

The Destination Field, bits R08 through R11, select one of 12 destination registers. Table 4-3 provides the Destination codes.

The ALU Control Field, bits R03 through R07 activate five of the six ALU control lines. The remaining ALU control lines, Cn is activated by a control flip-flop. Table 4-4 provides the ALU operation codes.

LOAD CONSTANT MICRO INSTRUCTION

The Load Constant micro instruction, identified by R13=0, R14=0 and R15=1, loads an 8 bit character (constant) originating from the PROM into one of 12 destination registers. Figure 4-13 shows the instruction format.

TABLE 4-1. SOURCE A CODES

SOURCES = R15 R14

R02	R01	R00	SOURCE A
0	0	0	(FILE) RAMS
0	0	1	(WORD COUNTER) WCS
0	1	0	(A-LINES LOW) AINLS
0	1	1	(A-LINES UP) AINUS
1	0	0	(B-REGISTER) BREGS
1	0	1	(Q-LINES) QS
1	1	1	(PROGRAM COUNTER) PCS

Source A is the ROM in Load Constant Instruction (R15, $\overline{R14}$, $\overline{R13}$).

TABLE 4-2. SOURCE B CODES

R13	R12	SOURCE B
0	1	(CWA_L) CWALS
0	0	(CWA_U) CWAUS
1	1	(BUF 2_L) BF2LS
1	0	(BUF 2_U) BF2US

Table 4-3. DESTINATION REGISTER CODES

DESTINATION NUMBER	R_{11}	FIELD R_{10}	R_9	R_8	DESTINATION
0	0	0	0	0	NOT USED
1	0	0	0	1	NOT USED
2	0	0	1	0	NOT USED
3	0	0	1	1	NOT USED
4	0	1	0	0	FILE ADDRESS REGISTER (RAMADD)
5	0	1	0	1	CWAuu (CPU MEMORY BANK) BANKD
6	0	1	1	0	FILE (RAMD)
7	0	1	1	1	PROGRAM COUNTER (PCD)
8	1	0	0	0	WORD COUNTER (WCD)
9	1	0	0	1	A REG UPPER (AOUTUD)
10	1	0	1	0	CWA LOW (CWALD)
11	1	0	1	1	CWA UP (CWAUD)
12	1	1	0	0	A REG LOWER (AOUTLD)
13	1	1	0	1	BUF 2 LOW (BF2LD)
14	1	1	1	0	BUF 2 UP (BF2UD)
15	1	1	1	1	B REGISTER (BREGD)

Table 4-4. ALU CONTROL CODE
INTER-REGISTER MICRO-INSTRUCTION

ALU CONTROL				LOGIC	ARITHMETIC	
S_3	S_2	S_1	S_0	M = 1	M=0, C_{in}=1	M=0 C_{in}=0
0	0	0	0	$\overline{A}$	A	A plus 1
0	0	0	1	$\overline{A+B}$	A+B	(A+B) plus 1
0	0	1	0	$\overline{A}\cdot B$	$A+\overline{B}$	$(A+\overline{B})$ plus 1
0	0	1	1	Logic 0	minus 1 (2s comp)	zero
0	1	0	0	$A\cdot B$	A plus $A\cdot\overline{B}$	A plus $A\cdot\overline{B}$ plus 1
0	1	0	1	$\overline{B}$	$A\cdot\overline{B}$ plus (A+B)	$A\cdot\overline{B}$ plus (A+B) plus 1
0	1	1	0	A+B	A minus B minus 1	A minus B
0	1	1	1	$A\cdot\overline{B}$	$A\cdot\overline{B}$ minus 1	$A\cdot\overline{B}$
1	0	0	0	$\overline{A}+B$	A plus $A\cdot B$	A plus $A\cdot B$ plus 1
1	0	0	1	$\overline{A+B}$	A plus B	A plus B plus 1
1	0	1	0	B	$A\cdot B$ plus $(A+\overline{B})$	$A\cdot B$ plus $(A+\overline{B})$ plus 1
1	0	1	1	$A\cdot B$	$A\cdot B$ minus 1	$A\cdot B$
1	1	0	0	Logic 1	A plus A=2xA	A plus A=2xA plus 1
1	1	0	1	$A+\overline{B}$	A plus (A+B)	A plus (A+B) plus 1
1	1	1	0	A+B	A plus $(A+\overline{B})$	A plus $(A+\overline{B})$ plus 1
1	1	1	1	A	A minus 1	A

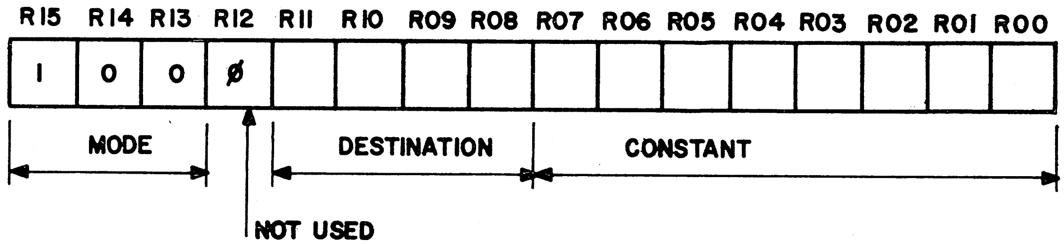


Figure 4-13. LOAD CONSTANT MICRO-INSTRUCTION FORMAT

Bits R08 through R11 select the destination register. Table 4-3 provides the destination register codes.

JUMP MICRO INSTRUCTION

Jump type micro instructions are identified by R15=0. Figure 4-14 shows the Jump Micro instruction format.

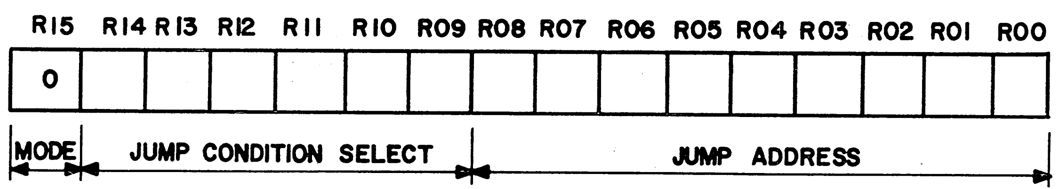


Figure 4-14. Jump Micro Instruction Format

R08 through R00 specifies the Jump Address. The 1K PROM is divided into 2 banks of 512 words each (locations 0-511 are called the lower bank, locations 512-1023 are called the upper bank). R08-R00 specify the address within a bank. The ROM bank Select (RMBNKS) F/F, which is set or reset by the Flip-Flop/Control Line Instruction, selects the bank to which the jump will be made.

The Jump condition select field consists of bits R14 through R09. There are seventy-two available jump conditions divided into two groups of sixty four and eight. The jump condition group (JGRP9) FNB FF, which is set or reset by the Flip-Flop/Control Line Instruction, selects the group. Bits R14-R09 select the condition within the group. (For the Group of 7, only R11-R09 are valid). Table 4-5 shows the Jump condition select codes and the corresponding jump conditions.

There are two types of Jump Instructions:

A) Unconditional Jump: This type is identified by R14-R09 equal zero. The program counter bits 0-8 will be loaded with R08-R00. Program counter bit 9 will be loaded with the contents of ROM Bank select (RMBNKS) F/F.

B) Conditional Jump: If the selected condition is true, the program counter will be loaded with R08-R00 and the Bank select (RMBNKS) F/F. If the selected condition is false, the program counter will be incremented by one.

Jumping to Subroutines

Jumping to subroutines is a two-step process. First the return address must be saved, and then a jump (conditional or unconditional) must be made to the starting address of the subroutine. (The bank select (RMBNKS) F/F must be set according to the bank in which the subroutine is located prior to the jump.) Figure 4-15 shows the instruction sequence necessary for jumping to and returning from subroutines. P incremented by one (P+1) is loaded into the register file at address 0 via an inter-register instruction. Address 0 is provided to the File Address Register (RAMADD) by the hardware. Execution of this instruction will also cause the upper two bits of the PC to be saved in flip-flops. Next, a jump is executed to the starting address of the subroutine. To return from the subroutine, zero is loaded into the File Address Register (RAMADD) via a load constant instruction. The contents of RAM 0 is incremented by one and loaded into the PC. This causes a jump to the return address (P+2). The upper two bits which were saved in flip-flops are loaded into the upper bit positions by hardware.

TABLE 4-5. JUMP CONDITION CODES

		R15	R14	R13	R12	R11	R10	R9	CDD	I/O PIN
JC	10	0	0	0	1	1	1	0	ALDENJC	(293)
	11	0	0	0	1	1	0	0	WTOP1JC	—
	12	0	0	0	1	0	1	0	SNSWDJC	—
	13	0	0	0	1	0	0	0	BLZROJC	—
	14	0	0	0	0	1	1	0	$\overline{\text{PRGPRT}}$	291
	15	0	0	0	0	1	0	0	RMEXEC	—
	16	0	0	0	0	0	1	0	SEEKER	92
	17	0	0	0	0	0	0	0	H (UCND JUMP)	—
JC	20	0	1	0	1	1	1	1	BUSBSY	99
	21	0	1	0	1	1	0	1	CRCERJC	—
	22	0	1	0	1	0	1	1	INDEX	93
	23	0	1	0	1	0	0	1	FRINXJC	(85)
	24	0	1	0	0	1	1	1	$\overline{\text{AUTOLD}}$	42
	25	0	1	0	0	1	0	1	—	(81)
	26	0	1	0	0	0	1	1	ONOFLN	—
	27	0	1	0	0	0	0	1	—	91
JC	30	0	0	1	1	1	1	1	LSTDT	—
	31	0	0	1	1	1	0	1	HFWRD	—
	32	0	0	1	1	0	1	1	CWAUL	35
	33	0	0	1	1	0	0	1	BF1F	—
	34	0	0	1	0	1	1	1	CWAUM	36
	35	0	0	1	0	1	0	1	$\overline{\text{WORD}}$	—
	36	0	0	1	0	0	1	1	$\overline{\text{FRSTDT}}$	—
	37	0	0	1	0	0	0	1	—	296
JC	40	0	0	0	1	1	1	1	EQUAL	—
	41	0	0	0	1	1	0	1	$\overline{\text{COUT}}$	—
	42	0	0	0	1	0	1	1	PRTFLT	237
	43	0	0	0	1	0	0	1	—	44
	44	0	0	0	0	1	1	1	BF2F	—
	45	0	0	0	0	1	0	1	PARERR	252
	46	0	0	0	0	0	1	1	ADRERR	263
	47	0	0	0	0	0	0	1	—	48

TABLE 4-5. JUMP CONDITION CODES (Contd)

		R15	R14	R13	R12	R11	R10	R9	CDD	I/O PIN
JC	50	0	1	1	1	1	1	0	ALDFXD	23
	51	0	1	1	1	1	0	1	ONCYL	24
	52	0	1	1	1	0	1	0	UNFDY	22
	53	0	1	1	1	0	0	0	—	25
	54	0	1	1	0	1	1	0	DKWTPT	16
	55	0	1	1	0	1	0	0	—	—
	56	0	1	1	0	0	1	0	—	21
	57	0	1	1	0	0	0	0	—	20
JC	60	0	1	0	1	1	1	0	ALTFRC	80
	61	0	1	0	1	1	0	0	DSKERR	—
	62	0	1	0	1	0	1	0	ALARM JC	—
	63	0	1	0	1	0	0	0	BMS$\overline{\text{D}}$	—
	64	0	1	0	0	1	1	0	WTOP2JC	—
	65	0	1	0	0	1	0	0	UNTPRT	—
	66	0	1	0	0	0	1	0	—	—
	67	0	1	0	0	0	0	0	SNGDNJC	—
JC	70	0	1	1	1	1	1	1	—	94
	71	0	1	1	1	1	0	1	SKCMPO	95
	72	0	1	1	1	0	1	1	SKCMP1	96
	73	0	1	1	1	0	0	1	—	297
	74	0	1	1	0	1	1	1	SKCMP2	97
	75	0	1	1	0	1	0	1	SKCMP3	298
	76	0	1	1	0	0	1	1	SECTOR	98
	77	0	1	1	0	0	0	1	—	299
JC	80	0	0	1	1	1	1	0	$\overline{\text{ONBUSJC}}$	—
	81	0	0	1	1	1	0	0	BL1JC	—
	82	0	0	1	1	0	1	0	—	10
	83	0	0	1	1	0	0	0	$\overline{\text{WCEMPT}}$	—
	84	0	0	1	0	1	1	0	—	—
	85	0	0	1	0	1	0	0	BMDL	—
	86	0	0	1	0	0	1	0	AUXJC	—
	87	0	0	1	0	0	0	0	COMPJC	—

TABLE 4-5. JUMP CONDITION CODES (Contd)

		R15	R14	R13	R12	R11	R10	R9	CDD	I/O PIN
JC	90*	0	0	0	1	1	1	0	—	295
	91	0	0	0	1	1	0	0	—	—
	92	0	0	0	1	0	1	0	MSW2	27
	93	0	0	0	1	0	0	0	—	—
	94	0	0	0	0	1	1	0	USNGDN	—
	95	0	0	0	0	1	0	0	MSW1	—
	96	0	0	0	0	0	1	0	NOCOMP	—
	97	0	0	0	0	0	0	0	—	—

*NOTE: JC Group 9 ENB P/P must be set.

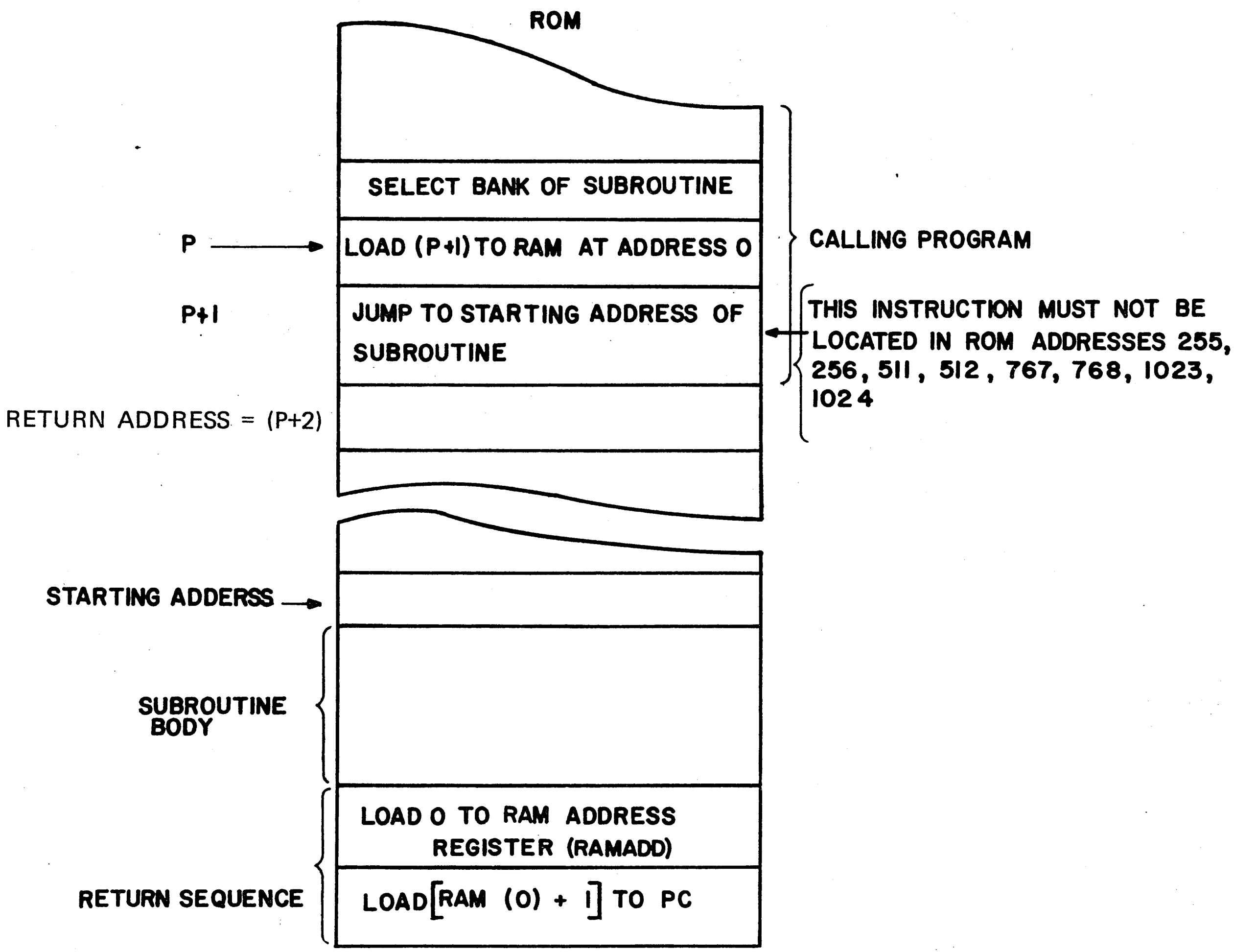


Figure 4-15. JUMP ROUTINE

The Jump Instruction which causes the jump to the starting address of the subroutine cannot be located in ROM addresses 255, 256, 511, 512, 767, 768, 1023, or 1024 due to the structure of the PC.

CONTROL LINE AND SET/RESET F/F INSTRUCTIONS

These instructions, identified by R13=1, R14=0 and R15=1, are used for setting or resetting one of the 56 available control flip-flops and for providing a pulse on one of 16 available control lines. Both of these operations can be performed in the same micro-instruction. Figure 4-16 illustrates the instruction format.

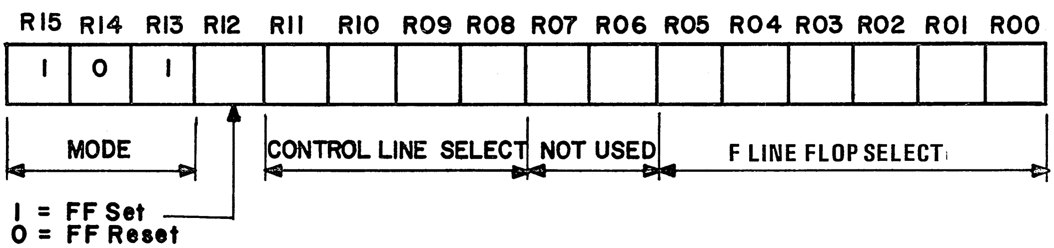


Figure 4-16. Control Line and Set/Reset F/F Instruction Format

The Flip-Flop Select Field, R00 through R05, selects one of 56 available flip-flops. Table 4-6 provides the flip-flop codes. Bit R12=0, resets the selected flip-flop. Bit R12=1 sets the selected flip-flop.

The Control Line Select Field selects one of 16 available control lines which will be strobed. Table 4-7 provides the control line codes.

TABLE 4-6. FLIP/FLOP CODES

FDD				R5	R4	R3	R2	R1	R0	CDD	I/O PIN
F/F	GRP	1	0	1	1	0	1	1	1	TRKOFS	5
			1	1	1	0	1	1	0	CASTRB	50
			2	1	1	0	1	0	1	——	8
			3	1	1	0	1	0	0	AUXFF	——
			4	1	1	0	0	1	1	RMBNKS	——
			5	1	1	0	0	1	0	BL1FF	——
			6	1	1	0	0	0	1	CABITO	7
			7	1	1	0	0	0	0	COMPOFF	——
F/F	GRP	2	0	0	1	0	1	1	1	SELBFI	——
			1	0	1	0	1	1	0	——	81
			2	0	1	0	1	0	1	——	294
			3	0	1	0	1	0	0	RTZS	82
			4	0	1	0	0	1	1	HS2	85
			5	0	1	0	0	1	0	——	86
			6	0	1	0	0	0	1	RDGATE	87
			7	0	1	0	0	0	0	SELBF2	——
F/F	GRP	3	0	0	1	1	1	1	1	WTRDMP	——
			1	0	1	1	1	1	0	BF1ENB	——
			2	0	1	1	1	0	1	ENBDB	——
			3	0	1	1	1	0	0	EGWG	250
			4	0	1	1	0	1	1	ENWDSY	——
			5	0	1	1	0	1	0	COMP1	——
			6	0	1	1	0	0	1	RWMOD	——
			7	0	1	1	0	0	0	CSFTRG	——

TABLE 4-6. FLIP/FLOP CODES (Contd)

FDD				R5	R4	R3	R2	R1	R0	CDD	I/O PIN
F/F	GRP	4	0	1	0	1	1	1	1	ALARMFF	—
			1	1	0	1	1	1	0	BUSY	—
			2	1	0	1	1	0	1	—	—
			3	1	0	1	1	0	0	DMWRPT	232
			4	1	0	1	0	1	1	CRCMOD	—
			5	1	0	1	0	1	0	FRCBUS	242
			6	1	0	1	0	0	1	JGRP9	—
			7	1	0	1	0	0	0	INTRSP	249
F/F	GRP	5	0	0	0	1	1	1	1	RQBUS 2	—
			1	0	0	1	1	1	0	COMP 2	49
			2	0	0	1	1	0	1	HSI	88
			3	0	0	1	1	0	0	ALDENFF	293
			4	0	0	1	0	1	1	ENBNED	—
			5	0	0	1	0	1	0	BLEROFF	—
			6	0	0	1	0	0	1	WTOP1FF	—
			7	0	0	1	0	0	0	SNSWDFF	—
F/F	GRP	6	0	1	0	0	1	1	1	—	—
			1	1	0	0	1	1	0	US1	9
			2	1	0	0	1	0	1	US2	3
			3	1	0	0	1	0	0	US3	10
			4	1	0	0	0	1	1	ONBUS FF	—
			5	1	0	0	0	1	0	RQBUS1	84
			6	1	0	0	0	0	1	US0	4
			7	1	0	0	0	0	0	CNALU	—
F/F	GRP	7	0	0	0	0	1	1	1	PRIOR	227
			1	0	0	0	1	1	0	WTOP2FF	—
			2	0	0	0	1	0	0	—	—
			3	0	0	0	1	0	0	—	—
			4	0	0	0	0	1	1	EOP	—
			5	0	0	0	0	1	0	SNGDNFF	—
			6	0	0	0	0	0	1	—	—
			7	0	0	0	0	0	0	CNTPRT	—

TABLE 4-7. CONTROL LINE CODES

C.L.	R11	R10	R9	R8	CDD
0	0	0	0	0	NOT USED
1	0	0	0	1	(SET REJECT) REJ
2	0	0	1	0	(SET REQ) DMAREQ
3	0	0	1	1	(SET REPLY) RPLY
4	0	1	0	0	(CRC ERR INIT) CRCERCL
5	0	1	0	1	(RESET REQ) CREQ
6	0	1	1	0	(SETFRC RLSE INX) FRINXCL
7	0	1	1	1	(READ ZEROES) RDZERO
8	1	0	0	0	(SET BUF 1 FULL) SBF1F
9	1	0	0	1	(SET BUF 2 FULL) BSF2F
10	1	0	1	0	(CLEAR BIT COUNT) CBITC
11	1	0	1	1	(RESET NETWORK) CNET
12	1	1	0	0	——
13	1	1	0	1	(CLEAR DMA ERR) CDMAER
14	1	1	1	0	(RESET WORD) CWORD
15	1	1	1	1	NOT USED

TABLE 4-8. FILE REGISTER USAGE

	RAM ADD REG				CDD
(0)	0	0	0	0	Return Address
(1)	0	0	0	1	SECTOR STAT
(2)	0	0	1	0	CYLINDER STAT_L
(3)	0	0	1	1	CYLINDER STAT_U
(4)	0	1	0	0	INT REQ REG
(5)	0	1	0	1	SCRATCH REG
(6)	0	1	1	0	ALARM STAT L
(7)	0	1	1	1	ALARM STAT U
(8)	1	0	0	0	BLOCK LENGTH L
(9)	1	0	0	1	BLOCK LENGTH U
(10)	1	0	1	0	CHECKWORD STAT L
(11)	1	0	1	1	CHECKWORD STAT U
(12)	1	1	0	0	INVERSE DISK STAT
(13)	1	1	0	1	TRUE SECTOR STAT
(14)	1	1	1	0	TRUE CYL STAT L
(15)	1	1	1	1	TRUE CYL STAT U

LOGIC DESCRIPTION

A/Q INTERFACE

INPUT-OUTPUT OPERATIONS

The necessary conditions for an A/Q Input or Output operation are as follows:

1. The equipment code must match the equipment number.
2. The W=0 field signal ($\overline{\text{WEO}}$) must be true.
3. The Read or Write signal, as required, must be active (low).

Equipment Identification

The equipment number is determined by four jumper plugs individually inserted into (or removed from) socket terminals marked Q7, Q8, Q9, and Q10 at location S8B. Inserting a jumper plug into the Q7 terminal, for example, selects a "1" for that bit. Removing a jumper plug from the Q8 terminal selects a "0" for that bit, and so on. The four hexadecimal bits of the equipment code are received from the computer on the $\overline{\text{ADR 8}}$, $\overline{\text{ADR 9}}$, $\overline{\text{ADR 10}}$, and $\overline{\text{ADR 11}}$ lines at pins 281, 282, 283, and 284 respectively. These four signals are compared with the equipment code jumper settings.

Comparison of Equipment Number and Equipment Code

The equipment code bits from the computer are compared to the equipment number jumper plug settings by a 4-bit magnitude comparator at S9. If the compared bits match and the $\overline{\text{WEO}}$ signal is low, (i.e., "A=B in" (S9-3) is high) the "A=B out" comparator output (S9-6) will go high. The high output obtained at S9-6 is the first condition necessary for the activation of the A/Q Interface Sequencer (high level at U4-1).

The W Field

The signal $\overline{\text{WEO}}$ must be low for Read or Write operation. If the W field = 0 condition exists, then $\overline{\text{WEO}}$ at pin 292 will be low. This signal is received and inverted to a high level by a Schmitt-Trigger inverter at T9-11/10; T9-10 is connected to Comparator "A=B in" input (S9-3).

The READ Signal

The third condition for a Read operation is an active (low) READ signal from the computer at pin 248 ($\overline{\text{READ SSTB}}$). If READ is active, then $\overline{\text{READ}}$ at H9-13 will be low, and the inverter output (READ BUF) will be high at H9-12). The signal READ BUF is connected to: the flip-flop "Data In" at T4-12, a "2 input positive-OR gate" at T5-9 and the A-Bus Selector at F8-6.

When READ BUF is high, the output of the OR gate at T5-8 will be high. This provides the second enable to the 3-input positive NAND gate at U4-2.

The WRITE Signal

The third condition for a Write operation is an active (low) $\overline{\text{WRITE}}$ signal from the computer at pin 290. If WRITE signal is active, then T9-3 will be low and the output of this inverter at T9-4 will be high. This output (T9-4) is connected to: an OR gate at T5-10, a three input positive AND gate at U4-10 and a positive two input NAND gate at R2-9.

For a Write operation, the output of the OR gate at T5-8 goes high and gives the second enable to U4-2.

SEQUENCER Enable

If the ON-OFF LINE switch (location L1) is in the "ON" position, the Sequencer at location U3 is able to initiate a sequence of pulses. The enable is affected by release of the clear input at U3-1.

The hardware uses a digital filter formed by two flip-flops of the Hex D type at location U6. When U4-12 goes high, the OR gate output (T5-11) will also go high. U4-12 is connected to U6-4; U6-5 will go high after 0 to 50 nanosec (the clock of U6 is 20 MHz). U6-5 is connected to U6-14; U6-15 will go high after an additional 50 nanoseconds. The result is that the signal at T5-13 will go high 50 to 100 nanoseconds after the leading edge of U4-12.

POWER-ON Reset

This circuit generates a reset pulse at Power-On. C32 is charged through R30; at this time the inputs T7-2 and U6-1 are low. NOTE: The UM1, UM2, UM3, and UM4 are external connection points.

The diode D1 is used to discharge the capacitor at Power-Off.

A digital filter is formed by two flip-flops U6-3/2 and U6-13/12. The $\overline{\text{Master Reset}}$ signal from pin 46 is received at G9-13 (Schmitt Trigger Inverter). When G9-12 is high, U6-3 and T6-5 will also be high. U6-2 will go high after approximately 50 nsec. If the $\overline{\text{MR}}$ signal at G9-13 is still active after the delay of 100 nsec, T6-6 will go low driving T7-3 low which will in turn generate a low level at T7-6. The $\overline{\text{GR}}$ signal (from T7-6) will drive U1-3 high generating the master reset pulse.

CLOCK Circuit

The controller incorporates a 20 MHz Crystal Controlled oscillator. The oscillator is built from Q1 and Q2 transistors, T7-9,10/8; T6-13,12/11 and T6-9,10/8 gates, Y1 crystal, capacitors and resistors.

Phase Generator

The 20 MHz is the clock input at U6-9. The flip-flop U6-6/7 and the NAND gate T6-1, 2/3 form the 20 MHz divider. The output is a 10 MHz clock, U5 is a Hex D-type flip-flop. The connections U5-5 to U5-6 and U5-7 through T3-13/12 to U5-4 form the first part of a phase generator. G2 is a Decoder Demultiplexer. The inputs 1A (G2-2) and 1B (G2-3) are connected to U5-5 and U5-7. G2-4, 5, 7 and 6 are the phase generator outputs, $\overline{\emptyset 0}$, $\overline{\emptyset 1}$, $\overline{\emptyset 2}$ and $\overline{\emptyset 3}$, respectively, as shown in Figure 5-1.

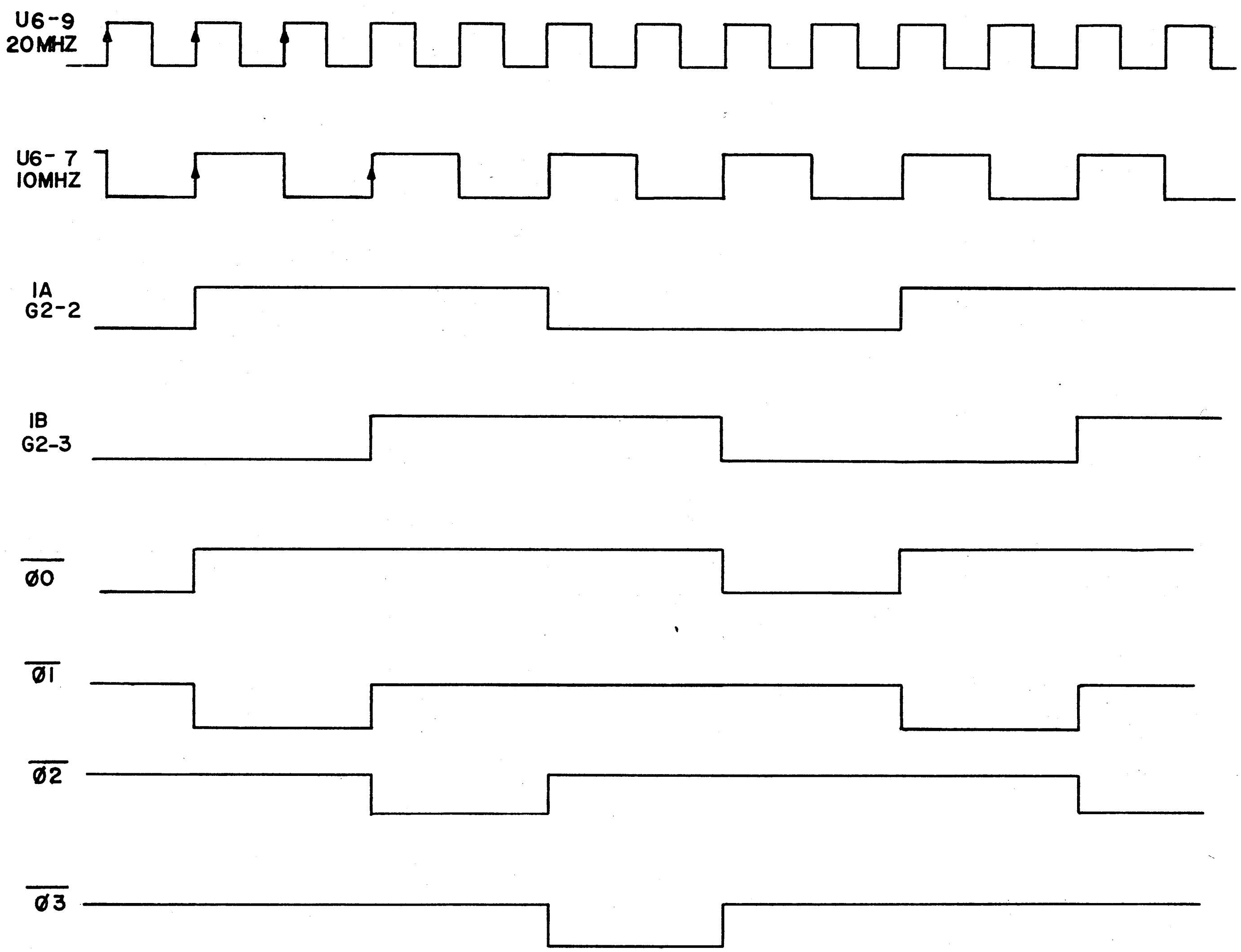


Figure 5-1. Phase Pulses

Phase pulses $\overline{\emptyset 0}$, $\overline{\emptyset 1}$, $\overline{\emptyset 2}$, and $\overline{\emptyset 3}$ have a pulse width of 100 nsec each.

Sequencer

Flip-flop U3 is the sequencer used for A/Q commands. Figure 5-2 shows the sequence.

The sequencer is clocked at 10 MHz.

When the controller receives an A/Q command (in the ON LINE state), the sequencer input U3-1 (clear) goes high.

The leading edge of the first 10 MHz clock pulse (U3-9) initiates the sequencer operation.

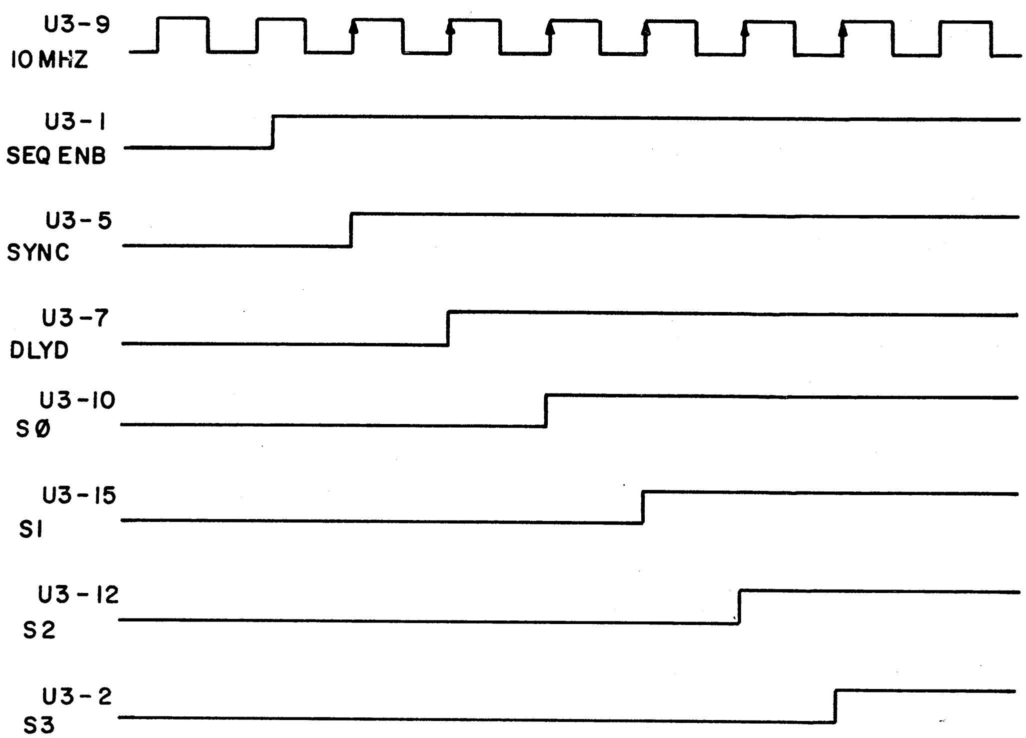


Figure 5-2. A/Q Sequence

When an immediate reject condition exists, the Controller generates the Reject signal at SO (U3-10) and the Sequencer stops, (a low level at U2-10 AND gate determines low at U3-14 Data Input).

If an immediate reject condition does not exist, SO causes the generation of S1 (U3-15).

Pulse S2 is generated when the A/Q command is a Clear Controller or a Read Dynamic Status command. For Clear Controller or Dynamic Status commands, $\overline{\text{ADR 5}}$ is low (thus making Q4 equal to 1), AND gate input U2-13 is high, and Data Input U3-13 (S1•Q4) is high.

If S1•Q4 is high, the sequencer generates pulses S2 and S3. The leading edge of pulse S3 generates the Reply pulse.

<u>REJECT Circuit</u>

The A/Q commands with Q4 = 0 ($\overline{\text{ADR 5}}$ = high) cause a reject condition if the controller is in the busy state. In this case, flip-flop BUSY (G1-5) is high, U2-5 is high, U2-4 is high, and AND gate output U2-6 is high. The flip-flop U6-11/10 and the AND gate U2-1,2/3 form a digital filter for the Q4 line.

Another condition for Reject is protect violation. If flip-flop C NTPRT (B1-12) is high, the controller is protected. An unprotected A/Q Write command causes a protect violation (U4-8 is high). Flip-flop T4-2,3/5 is the Reject flip-flop. A Reject condition (T4-2 high) causes the generation of the Reject pulse at the leading edge of SO.

It the A/Q command requires micro-program intervention, the program determines if and when the controller will send a Reject pulse to the CPU. In this case the control line $\overline{\text{REJ}}$ sets the Reject flip-flop (active low signal at T4-4). The reject pulse is transmitted to the CPU via driver B9-13,12/11 to pin 220.

REPLY Circuit

Flip-flop T4-12 11/9 is the Reply flip-flop. For A/Q commands with Q4=1, reply condition (T4-12 high) causes generation of the Reply pulse at the leading edge of S3. If the A/Q command requires micro-program intervention, the program decides if and when the controller will generate a Reply pulse. In this case, the control line $\overline{\text{RPLY}}$ sets the Reply flip-flop (active low signal at T4-10).

The Reply pulse is transmitted through driver B9-9, 10/8 to pin 218. The Reply and Reject circuits are enabled only at the time of an A/Q command (T4-13 and T4-1 are both high).

Micro-Program Execute Circuit

All A/Q commands with Q4=0 require micro-program intervention.

Flip-flop T2-12, 11/9 is the micro-program execute flip-flop. The leading edge of S1 sets the flip-flop when T2-12 is high (Q4=0).

The Clear Controller A/Q command (Q4=1) sets the RMEXEC flip-flop by an active low pulse at T2-10.

$\overline{\text{REJ}}$, $\overline{\text{RPLY}}$, or $\overline{\text{GR}}$ pulse reset the REMXEC flip-flop (T1-13 will be low through AND gate U4-3, 4, 5/6).

RMEXEC is connected as a Jump Condition (T1-14).

CONTROLLER Reset

The controller is reset by a $\overline{\text{GR}}$ pulse (T7-6) or by a Clear Controller A/Q command (Q4=1).

The Clear Controller generates an active low pulse at R2-8 (NAND gate). This pulse, like the $\overline{\text{GR}}$ pulse, generates a CCMR1 active high pulse at U1-3 driver output and a $\overline{\text{CCMR2}}$ and $\overline{\text{CCMR3}}$ active low pulse at J2-10 and J2-12 driver outputs.

A Clear Controller or $\overline{\text{GR}}$ pulse clears the Program Counter and activates the program from the first PROM address (000_{16}).

A-OUTPUT Register

The multiplexer with latched outputs at F4, E3, E4, and F3 form the A-Output Register. F4 and E3 store the eight least significant bits, and E4 together with F3 stores the most significant bits of the controller A-channel outputs. The ALU output bus is multiplexed with the Dynamic Status flip-flops at the input to the A-out register.

and the read signal will be active; S1·Q4 is high and the multiplexers select the Dynamic Status bits (F4-10, E3-10, E4-10, and F3-10 will be high) as the input to the A-Out register.

The exclusive-OR gate (R4-1, 2/3) generates the SPLS pulse. This pulse is transmitted through E2-9, 10/8 and E2-12, 13/11 NAND gates to clock the outputs of the Dynamic Status flip-flops into the A-Out register on the trailing edge of the SPLS pulse.

Under program control the clock for the A-Out upper and A-Out lower registers is generated by the destination decoder (k2-11 and K2-14 respectively) whenever the A-Out registers are selected as the destination registers by the micro-program.

A-OUT Register Buffer

The A-Out register outputs are driven by inverting three-state buffers at locations E5, F5, and B4. The buffers are enabled by output of the NAND gate at B3-6 which places the A-Out register contents on the A channel during A/Q read commands.

A-BUS Selector

The eight-bit A-Bus selector (F9, D9, F8, D8, D5, and C5) selects the A input to the ALU during the execution of an inter-register micro-instruction. The selector is composed of a 48-line to 8-line multiplexer with three-state outputs, 8-bit three-state buffer for the WC register, and the three-state outputs of the RAM. The A-Bus selector is controlled by the A-Source Decoder.

The following is a list of the inputs to the A-Bus Selector:

CPU A-Channel inputs lower	$\overline{SD1}$ - $\overline{SD8}$
CPU A-Channel inputs, upper	$\overline{SD9}$ - $\overline{SD16}$
CPU Q-Channel inputs	$\overline{ADR1}$- $\overline{ADR4}$, $\overline{ADR6}$, and READ BUF signal
ROM outputs PRO - PR7	
Program Counter bits 0 - 7	
B-Register outputs	
WC Register outputs	
RAM outputs	

A-Source Decoder

The A-Source Decoder consists of a selector at location A4 and a decoder demultiplexer at location B8. When a jump micro-instruction is executed, PR15 will be low. This will select the A input of the selector at A4, causing IR (from A4-9) to go low, and thus selecting PRO-PR7 as the outputs of the multiplexers at locations D5 and C5. Also the output of the AND gate (F2-6) will be driven low by the IR signal. This will enable the outputs of multiplexers D5 and C5 by placing a low signal on C5-15 and D5-15. Concurrently the IR signal will drive the inverter output at B2-12 high thus disabling the outputs of the decoder (B8). The decoder outputs B8-5, B8-6 will go high and will disable the outputs of the WC register buffers (C7-1, C7-15, and C6-15 will be high) and will disable the three-state outputs of the RAM (A6-8 and A7-8 will be high). With B2-12 high, the buffer outputs C6-9, 5, 3 and 7 will be disabled and will also be high. The function select pins of the ALU (GF7-6, 5, 4 and 3 and GF-6, 5, 4 and) will be high. The ALU M input (GF7-8 and GF6-8) will be driven high by NAND gate output B3-8. With S0-S3 and M inputs to the ALU high, the ALU will pass the PRO-PR7 data to ALU outputs GF7-9, 10, 11, and 13 and GF6-9, 10, 11 and 13.

For an inter-register micro-instruction, B2-12 is low. The B8 decoder is enabled and PRO, PR1 and PR2 provide the data for the decoder select inputs (B8-2, 3 and 14). When the selected source is the RAM B8-12 is low; A6-8 and A7-8 are low. When the word counter is the selected source, B8-11 is low C7-1, C7-15 and C6-15 are low.

PROGRAM COUNTER

Three synchronous 4-bit counters (D7, D6 and B5) provide a ten-bit address for the 1024 word PROM. This program counter receives its lower eight bits from the ALU-Out bus. The two most significant bits are loaded from a two-bit return address register which is used for returning from subroutines or from PRO8 and the output of the ROM bank select the flip-flop (RMBNKS). The multiplexer at A4 selects the input to the two most significant bits of the PC.

During a jump to Subroutine operation, the lower eight bits of the PC are saved in address 0 of the Register File (RAM) and the upper two bits of the PC are saved in the two-bit return address register at A3.

During subroutine returns, the upper two bits of the PC are loaded from the two flip-flops A3 by the selector A4. The lower 8 bits are loaded from RAM0.

Receipt of a low signal on the Load PC line (D7-9, D6-9 and B5-9) will cause the PC to be loaded on the trailing edge of $\overline{\emptyset 0}$. The PC outputs are connected to the PROM address and A-Bus selector.

PROM

The PROM is organized as an array of 512 words by 8 bits.

Four PROM's are used to construct a micro-memory of 1024 words by 16 bits.

The nine address bits of the PROM are provided by the nine lower Program Counter bits. The tenth bit of PC selects between the lower 512 word bank (CD1, CD3) and the upper 512 word bank (CD2, CD4). When B5-13 is low, the lower bank is selected (CD1-20, 21 and CD3-20, 21 are low); when B5-13 is high, the upper bank is selected (CD2-18, 19 and CD4-18, 19 are high). The 16-bit three-state outputs of the upper and lower PROM banks are wired-ORed together.

The PROM PRO-PR7 bits provide an A-source for the A-but selector. PROM bits are also connected to various circuits to generated and control micro-program execution.

B-REGISTER

The B-Register (locations E6 and E7) is a general purpose 8-bit register on the A-side of the controller. ALU-out bus data is multiplexed at the input to the B Register with receivers of input pins 29, 28, 37, 30, 33, 38, 31 and 34.

Flip-flop G1-6 selects the input to the B-Register. The trailing edge of $\overline{\text{BREGD}}$ pulse (from K2-6) strobes the selected data into the register. The B-Register outputs are connected to the A-Bus Selector. The B register 2^5 (BMDL) and B register 2^7 bits (BMSB) are connected to jump conditions at E1-14 and F1-1, respectively.

WORD COUNTER REGISTER

Two synchronous 4-bit Up-Down counters at B6 and B7 constitute the Word Counter Register. This circuit is used as an Up/Down Counter and as a general purpose register. When the Disk Controller executes a Read Data, Write Data, Compare Data or Checkword Check function, the WC Register counts the number of words per sector. The $\overline{\text{WCD}}$ pulse loads the Word Counters.

The counter counts down until $\overline{\text{WCEMPT}}$ (B6-13) goes low. This output is connected to E1-1.

The WC Register outputs are connected as an A-side source through three-state buffers at C7 and C6. Also, the WC-Register outputs are connected via drivers at A8A, C8B, C9B, A8A and C9A to pins 7, 18, 12, 14, 15, 19, 13, 17 and 11, respectively. This allows the WC to be used as a data to device register. For a Seek to Device command and a Load Disk Address command, the WC-Register sends a Cylinder Address to the device. The drivers are enabled and the Cylinder Address is placed on the lines only when the ONBUSFF flip-flop (A1-9) is set.

RAM

Two 16x4 clocked RAM's with three-state latched outputs (at A6 and A7) constitute the File of the Controller.

The address of the file is selected by a 4-bit RAM Address Register. The data to be written into the file is received from the ALU-out Bus.

The RAM three-state outputs are connected as a source to the ALU A-input.

An active low RAMD (from L2-9) pulse acts as a Write pulse at A6-2 and A7-2 during the time that A6-7 and A7-7 are held low. The timing diagram illustrates the operation mode of the file.

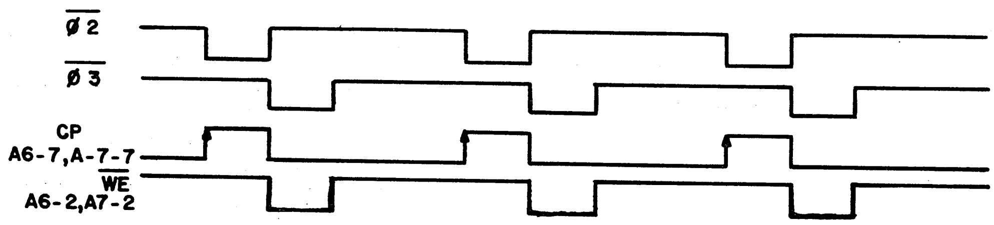


Figure 5-3. Timing for Operation Mode of File

The transition of CP from low to high causes the contents of the file location selected by the Address Inputs (A0-A3) to be strobed into the file Output Register. A three-state Output Enable ($\overline{EO}$) controls the Output Buffers. When $\overline{EO}$ (A6-8, A7-8) is low, the outputs are determined by the data in the output register.

RAM ADDRESS REGISTER

The Quadruple D-type flip-flops at A5 are used as the RAM Address Register. This register is loaded from the ALU-out bus with the address of the file register. The loading is executed on the trailing edge of $\overline{RAMADD}$ (L2-11) active low pulse.

ARITHMETIC LOGIC UNIT

The heart of the MP Device Controller consists of an 8-bit ALU (GF7 and GF6). The ALU is fed on the A-side by the A-Bus Selector which selects one of eight source A inputs. On the B side of the ALU, the B-Bus Selector selects one of the 4 source B inputs. The ALU-output bus is routed to one of 12 destination registers. The ALU performs sixteen binary arithmetic operations which are selected by four function-select lines (S0, S1, S2 and S3). The function select lines are received from the PROM through buffers (C6). These buffers are enabled during the execution of an inter-register instruction. In this case, the Data Selector/Multiplexer (A4) generates an IR signal: PR15 (A4-1) is high; PR14 (A4-10) is high; IR (A4-9 is high.

The IR signal is inverted by inverter B2-13/12 and provides an enable for C6-1.

The Internal Carry (GF7-7) is provided by flip-flop CNALU (A1-12). PR3 is enabled by the IR signal (B3-9) and inverted (B3-8). The output of the inverter supplies the input for the ALU (GF7-8, GF6-8).

The inverted Carry Output of the first ALU (GF7-16) is provided as a Carry Input to the second ALU (GF6-7).

Carry Out and A=B Latch

A 4-bit register at G5 is used as a latch for the ALU Carry Output (G5-2/4), for the ALU Comparator Output A=B (G5-1/6). During the execution of an inter-register micro-instruction, the IR signal will be high. This will cause the latch load input (G5-9) to be high. Data is strobed into the latch with the leading edge of clock phase $\overline{00}$. The latch data will remain valid until a new inter-register instruction is executed.
NOTE: the A=B ALU open collector outputs (GF7-14 and GF6-14) are wired OR together to give comparison for eight bits. A pull-up resistor $S3_2$ is used for the wired OR connection.

B-BUS SELECTOR

The Dual 4-line-to-1-line Data Selectors/Multiplexers at J9, J8, J7 and J6 constitute the B-Bus Selector. The B sources are CWA (Current Word Address Register) Low, CWA Up, Buffer 2 Low and Buffer 2 Up. The PROM bits PR12 and PR13 select the B-side source during the execution of inter-register micro-instructions.

The B-Bus Selector outputs are connected to the ALU B-inputs.

CURRENT WORD ADDRESS REGISTER

The synchronous 4-bit Up-Down counters K9, K8, K7, K6, and L6 constitute the CWA Register. This register is divided into three sub-registers: CWA_L (K9, K8), CWA_{up} (K7, K6), and Bank (L6). The inputs of each sub-register are connected to the ALU-out bus. The CWA_L and CWA_{up} outputs provide the inputs for the B-side selector. The two-bit bank outputs (L6-3 and L6-2) are connected as Jump Conditions to M1-2 and M1-15 respectively.

The CWA Register is used as an 18-bit address register during DMA Data Transfers. This register provides the sixteen bits of Memory Address and two bits of Memory Bank Address through buffer gates to the DMA Address pins. The sixteen address bits and the least significant bit of Bank Address are enabled by a signal that is the result of a logical AND between the $\overline{\text{REQACC}}$ pulse and the state of the Jumper Mode (inserted or removed). When the Controller executes a DMA Transfer cycle, the $\overline{\text{DMA-RA}}$ active low pulse enables the three-state buffer inverters L7, L8, and L9 (G4-1, 14/13 and J3-12, 13/11); L7-1, L7-15, L8-1, L8-15, L9-1, and L9-15 are low. The address bits $\overline{\text{DMA-MAB01}}$ to $\overline{\text{DMA-MAB17}}$ are connected at pins 53 through 62, 253 through 258, and pin 35.
NOTE: In the CDD Controller, the Jumper Mode state is always high (the jumper is removed). The memory bank address most significant bit is provided by L6-2 through buffer gate N9-14/13 to pin 36 ($\overline{\text{DMA-MAB18}}$). The $\overline{\text{DMA-MR}}$ active low signal enables this memory bit during the DMA Transfer cycle.

All of the Memory Address bits are active low signals.

The CWA Sub-registers are loaded from the ALU-out Bus. The CWA_L is loaded when an active low $\overline{\text{CWALD}}$ pulse from K2-13 is provided to K9-11 and K8-11. The CWA_{up} is loaded when an active low $\overline{\text{CWAUD}}$ pulse from K2-12 is provided to K7-11 and K6-11.

The Bank is loaded when an active low $\overline{\text{BANKD}}$ pulse from L2-10 is provided to L6-11. Loading of the CWA registers is done asynchronously with the register clock.

The clock for the CWA Register/Counter is the $\overline{\text{REQ ACC}}$ pulse with incrementation of the CWA registers taking place on the trailing edge of the $\overline{\text{REQ ACC}}$ pulse. Each time that a DMA cycle is completed, the counter is clocked and the address for the next DMA Transfer cycle is prepared. At the start of the DMA Transfer operation, the CWA Register is loaded with the First Word Address from the ALU-output bus.

DOUBLE BUFFER

1. BUFFER 1 REGISTER

The Buffer 1 Register is composed of four 4-bit registers with multiplexed inputs at M8, N8, P8 and R8. The 16 memory data bits from DFM01 to DFM16 from pins 264 to 279 are multiplexed at the input of the Buffer 1 register with 16-bit parallel data from the Shift Register of the Double Buffer. Flip-flop S5-4 selects the input to Buffer 1 and the loading is controlled by the Double Buffer Control. Data is strobed into the register on the trailing edge of the CLK BUF 1 pulse. The outputs of Buffer 1 are connected to the inputs of Buffer 2.

2. BUFFER 2 REGISTER

The Buffer 2 register is composed of four 4-bit registers with multiplexed inputs at M7, N7, P7 and R7. The register is divided into two-8 bit sub-registers called Buffer 2 low (bits 7-0) and Buffer 2 up (bits 15-8). Bits 15-8 of the Buffer 1 register are multiplexed with the ALU-output bus at the input of Buffer 2 up. Bits 7-0 of the Buffer 1 register are multiplexed with the ALU-output bus at the input to Buffer 2 low. Flip-flop S5-12 selects the input to Buffer 2 low and Buffer 2 up. The loading of Buffer 2 is controlled by the Double Buffer Control.

The outputs of the Buffer 2 Register are connected as sources (Buffer 2 Low - M7 and N7 and Buffer 2 Up - P7 and R7) to the B-side Selector. Also the Buffer 2 Register is connected through Buffer gates to $\overline{\text{DMA Data to Memory}}$ pins. The three-state bus drivers at R9, P9 and N9 transfer and invert the Buffer 2 Register data. These buffer gates are enabled by active low pulse $\overline{\text{STB-DTM}}$ from the DMA transfer control. The outputs of the buffer gates $\overline{\text{DMA-DTM01}}$ through $\overline{\text{DMA-DTM16}}$ are connected to pins 64 through 79. The Double Buffer Control Circuit provides separate clocks for the Buffer 2 Sub-registers. The clock for Buffer 2 Up is provided through K5-13, 12/11 and the clock for Buffer 2 Low is provided through K5-10,9/8.

3. SHIFT REGISTER

The Shift Register is composed of four 4-bit shift registers at M6, N6, P6 and R6. The shift register is used in the CDD Controller for a serial-to-parallel and parallel-to-serial data transfer conversion. The parallel input to the shift register is connected to the Buffer 2 output. The parallel output from the shift register is multiplexed at the input of the Buffer 1 Register with data from the DMA. The serial input to the shift register consists of the Read Data (serial) received from the disk. The serial output of the shift register is transmitted to the device as Write Data (serial) through a Transmitter circuit.

The shift register is cleared when flip-flop CSFTRG (N1-12) is in the reset state. For the shift register to work, flip-flop CSFTRG must be high. The clock to the shift register is provided by the selector (P3) which chooses between the Read Clock and the $\overline{\emptyset 0}$ clock phase.

The loading of the shift register is accomplished by a low level at M6-9, N6-9, P6-9 and R6-9.

The activity of the shift registers is controlled by the micro-program. During a Write-to-Disk operation, the shift register is loaded with data from the memory or data from the ALU through the Buffer 2 register. An internal clock is provided to M6-10, N6-10, P6-10, and R6-10. The RWMOD flip-flop (N4-11) is high (Write). The clock phase $\overline{\emptyset 0}$ is transferred through the multiplexer at P3 and through a driver-inverter (F5-14/13) to the shift register clock. Synchronous loading is enabled by a low level at L5-8. When the Bit Counter has counted a 16_{10} bit word, the signal $\overline{\text{Word Sync}}$ (M4-2) goes low and enables shift register loading. A new 16_{10} bit word is loaded into the shift register from the Buffer 2 Register on the trailing edge of clock pulse $\overline{\emptyset 0}$. The shifted data is received by the Write Data Transmitter (R6-12), passes through the selector (P3-6/7) and the inverter (T3-9/8), and appears at the input of the CRC and Write Data Transmitter circuits. When the Controller reads data from Disk and transfers it to the Memory or to the ALU, the shift register transforms the serial data to parallel data. The Read Data is received from pin 89 through T9-5/6 receiver, Read Data Extender circuit (K4 flip-flops and T5 and L5 OR gates), P3 Selector, and T3-9/8 inverter. The Read Data is connected to the First State Input of the Shift Register (M6-2,3) and after sixteen shifts is transferred in parallel form to the Buffer 1 Register. This transfer is controlled by the Double Buffer control.

If a Write to Memory operation is required, the data is transmitted through buffer gates to DMA-DTM pins.

The parallel data from Buffer 2 can be transferred to other controller registers through the B-side Selector and the ALU.

4. DOUBLE BUFFER CONTROL

The Buffer 1 full signal is generated by the J-K negative-edge-triggered flip-flop at location L4. The flip-flop is clocked by the CLK BUF 1 signal. The CLK BUF 1 signal is generated whenever a DFM (Data From Memory) strobe is received from the DMA control, or when 16 bits of serial data from the disk have been received in the shift register. The program must set the BF1ENB (N1-5) flip-flop in order to allow the J input (L4-9) of the Buffer 1 Full flip-flop to be high.

The enable for Double Buffer activity is provided by ENBDB flip-flop (N1-6). When this flip-flop is high, L4-8, L4-3, J4-8, and J4-3 are high allowing the flip-flops to be set.

The output of Buffer 1 Full flip-flop (L4-11) is connected to a BF1F Jump Condition (M1-1) and to the J-input of the Lost Data 1 flip-flop (L4-4). If a CLK BUF 1 is provided when BUF 1 FULL flip-flop is set (Buffer 1 Register is full), then the flip-flop Lost Data 1 will be set. The Lost Data S/R flip-flop output is connected to a LSTDT Jump Condition at M1-4.

The J-K negative-edge-triggered flip-flop (J4-9, 12, 6/11) comprises the Buffer 2 Full flip-flop. J4-4, 16, 1/14 comprises the Lost Data 2 flip-flop.

The automatic control of the Double Buffer is based on the $\overline{\text{CLK REQ}}$ generator. When the Buffer 1 Register and the Buffer 2 Register are empty, L5-1 is high and L5-2 is low. The result is that L5-3 is high. Two flip-flops, K4-13/12 and K4-11/10, are cascaded (K4-12 to K4-11). These flip-flops are clocked by the 10 MHz clock.

While L5-3 is high, the K4-10 output is high, M4-5 is high, and J3-5 will be high. When L4-11 goes high, L4-10 goes low, L5-3 goes low, and K4-13/12, 11/10 produces a 200 nsec active low pulse. This pulse, which is named $\overline{\text{CLK REQ}}$, resets the Buffer 1 Full flip-flop and sets the Buffer 2 Full flip-flop. After this J4-11 goes high, L5-3 goes high, and K4-10 goes high.

The $\overline{\text{CLK REQ}}$ active low pulse passes through NAND gates at K5 and appears as a strobe pulse at the Buffer 2 Register clock inputs (M7-11, N7-11, P7-11 and R7-11).

If the Buffer 2 Register is full, J4-11 is high. In this case, if a CLK BUF 1 pulse is received, a $\overline{\text{CLK REQ}}$ pulse will not be generated. The Buffer 1 Register is loaded and BUF 1 Full flip-flop is set (L4-11 goes high). A new CLK BUF 1 pulse will cause a lost data condition and will set the lost data flip-flop.

When the Buffer 1 Full flip-flop is reset, (L4-10 is high) and Buffer 2 Full flip-flop is set, (J4-11 is high), i.e., Buffer 1 is empty and Buffer 2 is full, a CLK BUF 2 pulse will reset the Buffer 2 Full flip-flop and J4-10 will go high. A CLK BUF 2 pulse when J4-10 is high determines Lost Data (J4-14 goes low and M3-4 goes high).

The micro-program resets the S/R flip-flop at M3-1, 2, 3/4 via the Control Line $\overline{\text{CNET}}$ (M2-12). When no memory transfer operations are in progress, the Controller can utilize the BUF 1 Full flip-flop and the BUF 2 flip-flop as Index flip-flops (flip-flop connected to Jump Condition). In this case, $\overline{\text{SBF1F}}$ (M2-15) sets BUF 1 Full flip-flop (L4-7) and $\overline{\text{SBF2F}}$ (M2-14) sets BUF 2 Full flip-flop (J4-7). The BUF 1 Full flip-flop output is connected to Jump Condition M1-1 and the BUF 2 Full flip-flop output is connected to Jump Condition H3-15. These two indexes are reset by the resetting of the ENBDB flip-flop.

CRC CIRCUIT

The Cyclic Redundancy Check Generator/Checker at N5 is a 16-bit programmable device which operates on serial data streams and provides a means of detecting data errors.

The CRC circuit consists of a CRC Generator/Checker at N5, two D-type flip-flops at P5, two J-K positive-edge-triggered flip-flops at S4 and a 2-input AND-OR-invert gate at M5-2,3,4,5/6. When the controller writes data to the device, the CRC circuit generates a 12-bit polynomial which is input to the Write Data Transmitter following the data block. When the Controller reads an address or data from device, the CRC Circuit checks the data and compares it with the 12-bit CRC polynomial. Detected errors are latched. The CRC Generator/Checker receives its clock at N5-1 and its data at N5-11. A 3-bit control input selects one of eight generator polynomials. These inputs are N5-3 (high), N5-5 (high), and N5-8 (low). The Data Output N5-12 is connected to M5-3. After the Address or Write Data transmission is completed, the D-type positive-edge-triggered flip-flop (P5-2,3/5) enables the transmission of the CRC polynomial. When the controller is transmitting data, the flip-flop CRCMOD (G1-9) is reset by the micro-program after which P5-4 is low and P5-5 is high. N5-10 will be high and the data is received. After the last data bit is received, N5-10 goes low and the check bits are shifted out of the register and appended to the data bits using external gating. The program sets CRCMOD flip-flop and P5-5 goes high. With a new $\overline{\text{Word Sync}}$ active low pulse, the P5-2,3/5 flip-flop is reset. At the trailing edge of $\overline{\text{Word Sync}}$, P5-5 goes low followed by N5-10 going low.

When P5-5 is high, Data transmission is enabled. M5-5 being high determines that inverted data shall appear at M5-6.

When P5-5 goes low and P5-6 goes high, the Data transfer is interrupted and the CRC polynomial transfer is performed via M5-2,3,4,5/6 gate.

The CRC generation/checking is initiated by the First of Data pulse which causes N5-4 to go high asynchronously clearing the CRC register.

When the Bit Counter L3 has counted a 1/2 word (eight bits of the word), the micro-program prepares the circuit for the receipt of a 1/4 word (four bits). A 1/4 word signal after the 1/2 word signal (HFWRD) indicates that 12 bits have been counted.

For a compare operation it is necessary to make use of the 1/4 word signal delayed. The 1/4 word signal is connected to S4-2 and S4-3 (J-K positive-edge-triggered flip-flop). Control Line CRCERCL (S2-11) resets the flip-flop output S4-6 and sets the flip-flop S4-14,13,12/9. The micro-program activates the CRCERCL Control Line when the HFWRD signal is detected during receipt of the CRC polynomial The CRC circuit is now prepared to latch the CRC Error Output. The low-to-high transition at S4-9 constitutes a clock for the P5-12,11/9 flip-flop. For a CRC Error, a high level is generated at N5-13, the low-to-high transition latches the error into P5-12,11/9 and jump condition CRCER (R1-3) goes high.

FIRST OF DATA CIRCUIT

The micro-program controls the detection of the first bit of data (or the first bit of address). The operation is initiated by an active low pulse at $\overline{\text{RDZERO}}$ (S2-7) which sets the flip-flop M3-15,14,13. The N3-1 flip-flop is released and the N3-2,3/5 flip-flop is enabled. The data is connected to N3-2. While the data bits are zero, the flip-flop output N3-5 is low, N3-6 is high, and K4-5 and K4-7 are high. The pulse width generator for the First of Data circuit consists of the two D-flip-flops K4-4/5 and K4-6/7.

A "one" data at N3-2 causes a low level at N3-6 followed by a low level at K4-7 after a 100-200 nsec time interval. The low level at K4-7 resets the flip-flop M3-15,14/13. The N3-1 (reset) is released and the N3-2, 3/5 flip-flop is enabled.

The active high pulse at N3-5 indicates the detection of the First bit of Data.

WRITE DATA TRANSMITTER

The Write Data is inter-mixed with the clock and transmitted to the device. The OR gate L5-4,5/6 produces the data pulses by OR-ing between $\overline{\text{Ø3}}$ and $\overline{\text{Data}}$. NAND gate K5-4,5/6 provides the mixed data for transmission. The $\overline{\text{Ø3}}$ clock phase is used for mixing.

Flip-flop ENWDSY (N1-9) enables transmission by a high level at K5-1.

The enable at J5-1 for the Peripheral Driver J5-1,2/3 - 4/5 is provided by resetting flip-flop COMP2 (S1-5) through the NAND gate R2-1,2/3. The Driver includes a filter network R14, C27, R13 to improve the form of the transmitted signal. Signal $\overline{\text{Write Data}}$ is connected to pin 49.

READ DATA

The Data is received by a Schmitt-Trigger inverter T9-5/6 and extended by two flip-flops and gates. The Output of the OR gate at L5-11 is at a high level during the reception of a high level at T9-6. The flip-flops K4-3/2 and K4-14/15 are clocked by the 10 MHz clock. The outputs of the flip-flops are connected to OR gate T5-4,5/6. T5-6 is connected to OR gate L5-13,12/11. In this mode, the Read Data pulse is extended by 50-100 nsec.

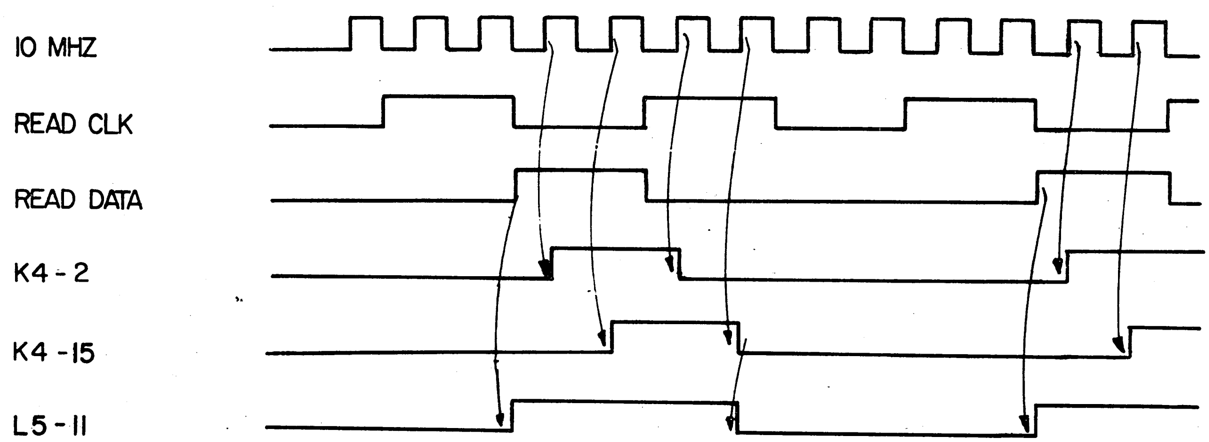


Figure 5-4. Read Data Extended

BIT COUNTER

The Bit Counter (L3) is provided with a clock input (L3-2) that is selected by the multiplexer at P3. A high level at L3-15 indicates that the counter has counted 15 clocks. To extend the clock counting to 16 clock pulses, the carry output of the bit counter (L3-15) is connected to the Data input of the D-flip-flop at N3-12. This carry out extension is controlled by the micro-program. Flip-flop ENWDSY (N1-9) enables Word Sync flip-flop activity (N3-13 will be high when flip-flop ENWDSY is set). The OR gate output at K3-8 provides the active low $\overline{\text{Word Sync}}$ pulse. This pulse indicates that a word (16-bits) has been transferred or compared. The

$\overline{\text{Word Sync}}$ active low pulse activates (resets) the $\overline{\text{Word}}$ flip-flop.

The output of this Set/Reset flip-flop at M3-9 is connected to jump condition M1-14 and provides word transfer information to the micro-program. This flip-flop is deactivated (set) by control line $\overline{\text{CBITS}}$ from M2-13, which also clears the bit counter, or by control line $\overline{\text{CWORD}}$ (M2-9).

The $\overline{\text{Word Sync}}$ active low pulse activates (resets) the $\overline{\text{Word}}$ flip-flop. Flip-flop COMP1 is connected to the preset enable of the bit counter (L3-3). When the controller executes a Compare operation, flip-flop COMP1 is set high and the counter is loaded with the constant "0001". When the Controller executes a Read operation, the counter is loaded with "0000". For a Write operation, the counter Load function is disabled. Flip-flop RWMOD (N1-11) is high for a Write operation causing L3-9 to be high and disabling the load function through OR gate output K3-6.

When flip-flop RWMOD is low, the First of Data pulse (active high) from M3-13 is inverted by the NAND gate at R2-6 and causes a load into the Bit Counter.

READ/WRITE/COMPARE SELECTOR

The two multiplexers at P3 and P4 select clocks and strobes for the various double buffer operations. Flip-flop RWMOD is connected to P3-1 and flip-flop COMP1 is connected to P4-1. P3-2,3/4 selects the clock between Read Clock and $\overline{\text{Ø0}}$. P3-5,6/7 selects the data between the Read Data extender and Serial Data to be written on to the Disk. The selectors at P3 and P4 provide the CLK BUF 1 and CLK BUF 2 pulses for the Double Buffer. The input signals to these selectors are the MDA data transfer cycle pulses (STB-DTM and STB-DFM) and the $\overline{\text{Word Sync}}$ pulse from the Bit Counter. P4-5,6/7 is used as an inverter gate.

COMPARE CIRCUIT

When the controller executes a compare operation. The micro-program sets the necessary flip-flops. P3-1 is low which allows the selector to select the Read Clock and the extended Read Data. Flip-flop COMP1 is set; thus the clock for Buffer 1 (CLK BUF 1) comes from the STB DFM pulse and the clock for Buffer 2 (CLK BUF 2) comes from the Word Sync pulse.

Each Word Sync pulse provides a loading pulse to the shift register of the Double Buffer through M4-1,2/3 and L5-9,10/8. The First of Data pulse initiates the Compare operation. The Bit Counter is loaded with "0001" through R2-4,5/6 NAND gate and K3-4,5/6 OR gate by the First of Data pulses. The Compare Circuit consists of J-K positive-edge-triggered flip-flop (N4), the jump condition NOCOMP (J1-13), two AND gates, and an exclusive OR gate. The flip-flop N4-2,3,4/6 is the Enable Compare flip-flop. The resetting of this flip-flop is executed by the activation of Control Line CNET (M2-12). For a Compare operation, flip-flop COMP 2 is reset by the micro-program causing R2-3 to go high thus setting the enable compare flip-flop on the trailing edge of the Word sync pulse.

The exclusive OR gate R4-4,5/6 compares the Read data (R4-5) with the data from Memory. The data from Memory is transferred by the Double Buffer to the shift register which transmits serial data to R4-4. The output of the exclusive OR (R4-6) is enabled by a high level at M4-9. M4-8 is connected to N4-14. The Read clock is connected to N4-12. The micro-program sets the flip-flop COMP2 (S1-5) one word before the end of the data comparison. The last Word Sync pulse resets the Enable compare flip-flop (N4-2,3 is low and Word Sync clocks the flip-flop through the AND gate at M4-11.

The program checks the jump condition MOCOMP to determine if the comparison was successful. N4-14,12/10 is reset by the control line CNET (an active low pulse).

DMA TRANSFER CONTROL

The DMA data transfer is controlled by a circuit which provides the DMA-Memory Request signal, receives the DMA-Request Accept signal, and commands the direction and the timing of the data transfer and of the function transfer (protect, errors).

The micro-program sets the ENBNED flip-flop (S1-9) and enables the Request flip-flop (T2-2 will be high). The clock for this flip-flop is provided by the Double Buffer Control Network (K4-10). The request flip-flop can also be set by the Control Line DMAREQ (S2-13).

When flip-flop ENBNED is set, the CLK REQ sets the Request flip-flop. T2-6 goes low and drivers N9-12/11 and N9-14/13 are enabled causing the $\overline{\text{DMA-MR}}$ to go active (low) at pin 260 and $\overline{\text{MDA-MAB18}}$ to be enabled at pin 36.

When the CPU Memory Control is able to receive or to transmit memory data, the signal $\overline{\text{DMA-RA}}$ (low active) is received by the controller at pin 261. This signal enables the bus driver at G4.

The low level at G4-13 ($\overline{\text{REQ ACC}}$) resets the DMA Request flip-flop T2-2,3/5 through the AND gate (J3-1,2/3). The control line $\overline{\text{SREQ}}$ is also used to reset the DMA Request flip-flop when it is necessary to terminate a DMA request due to the detection of an error.

The DMA WRITE signal is transmitted at pin 63. This signal is generated by the micro-program which controls flip-flop WTRDMP (N1-4). The output of this flip-flop is inverted and buffered by G4-12/11. The flip-flop WTRDMP is also connected through inverter G3-11/10 to G4-4. The $\overline{\text{STB DTM}}$ pulse (active low) appears at the output of G4-5. This pulse enables a Data Transfer to the Memory (R9-1, R9-15, P9-1, P9-15, and N9-1 go low). The inverter (T3-5/6) provides the STB DTM signal to the double buffer through the Read/Write/Compare selector. The $\overline{\text{DMA PROT}}$ signal is generated from G4-3. The micro-program sets flip-flop DMWRPT (G1-7). When a $\overline{\text{DMA-RA}}$ signal is received, the controller transmits a $\overline{\text{DMA-PROT}}$ signal at pin 232.

The $\overline{\text{DMA-MDS}}$ active low pulse is received at pin 262 whenever the controller receives data from the memory. The DMA-MDS pulse is received by a Schmitt-Trigger receiver at G3-13/12 and transferred through G4-6/7 to the Read/Write/Compare selector as the $\overline{\text{STB DFM}}$ active low pulse. This pulse indicates the availability of memory data to the controller.

The controller receives the $\overline{\text{DMA-MPE}}$ (parity error), $\overline{\text{DMA-PFLT}}$ (protect fault) and $\overline{\text{DMA-MAE}}$ (address error) at pins 39, 237, and 263 respectively. OR gates at H6 enable these signals to be latched into three shift register flip-flops at H5. Whenever the $\overline{\text{REQ ACC}}$ signal is active, H6-12,2,10 will be low allowing the memory error signals to be transmitted to the latch inputs (H5-1,2,6,15). The control line $\overline{\text{CDMAER}}$ (from M2-10) resets the memory error latches under micro-program control.

To attempt to prevent Lost Data, the controller generates a $\overline{\text{PRIORITY}}$ signal at pin 227. This signal is activated when the micro-program sets flip-flop Priority (B1-4). The Priority signal is enabled by the Request flip-flop (whenever M9B is high).

DUAL ACCESS TO THE DEVICES

The controller incorporates provisions for dual CPU access to the devices. The $\overline{\text{BUS BUSY}}$ signal, received at pin 99, is active (low) when the second controller has control of the bus. Jumper Double Bus (SB) is inserted for dual access. The $\overline{\text{BUS BUSY}}$ signal is received by U8-13/12 and transferred (inverted) to jump condition BUSBSY (R1-4).

The normal state of flip-flop RQBUS2 (S1-4) is high, thus the output at U1-6 is low.

The jumper Simultaneous Bus Determine (BP) is inserted or removed to determine which controller will gain bus control in the case of both controllers attempting to connect onto the bus simultaneously. Control will go to the controller which has the jumper removed.

If the controller has higher priority, the Simultaneous Bus Determine jumper is removed and the driver S8A-2,1/3 receives an Enable (S8A-2 is high). Flip-flop RQBUS1 (A1-10) announces that the controller wants to connect onto the bus. If both controllers set their RQBUS1 flip-flop, both controllers will generate a $\overline{\text{BUS NEED}}$ active low signal at pin 84. The Bus Busy signal is received (active low) at pin 99 of the respective controller. U1-6 will go low in both of the controllers.

In the controller which has the simultaneous Bus Determine jumper inserted, S8A-2 will go low and the $\overline{\text{BUS NEED}}$ signal will be deactivated (pin 84 will go high). In this mode, the controller without the jumper will remain on the bus.

For a normal Bus Connect operation, the controller transmits the $\overline{\text{BUS NEED}}$ signal to the second controller. The micro-program resets the flip-flop RQBUS2 (U1-6 will go high). The program sets flip-flop RQBUS1 (S8A-3 will go low). When the alternate controller releases the bus, the first controller may connect onto it.

The controller can gain immediate bus control by forcing the alternate controller of the bus. Flip-flop FRCBUS (G1-10) through the inverter (J2-3/4) generates the $\overline{\text{Force Bus}}$ signal to the alternate at pin 22. The controller can be forced off the bus by the alternate in the following manner: At pin 80 the $\overline{\text{Alt Force}}$ active low signal is received. This signal is transferred by a Schmitt-Trigger inverter G3-9/8 and will cause the input of the NAND gate (B9-5) to go high. At the same time, the alternate controller will provide a $\overline{\text{Bus Busy}}$ active low pulse at pin 99, causing B9-4 to go high. The output B9-6 will generate a Master Clear active low pulse through AND gate T7-5,4/6.

The D-flip-flop (R3-4,1/5) is used as the force bus release index. The micro-program sets this flip-flop via control line FRINXCL (S2-9). This flip-flop informs the micro routines that the alternate controller has forced the release of the device bus. This index is reset by control line CRCERCL (S2-11).

DESTINATION DECODER

The Decoder/Demultiplexers L2 and K2 make up the Destination Decoder. The select inputs L2-1,2,3 and K2-1,2,3 are connected to PR8, PR9 and PR10. $\overline{\text{PR11}}$ enables L2-6 and PR11 enables K2-2 (thus choosing between the two decoders); $\overline{\text{Dest Decoder}}$ Enb from AND gate (F2-8) enables L2-5 and K2-5. The active low pulse to clock the selected destination is generated when the clock phase Ø3 enables the L2-4 and K2-4 decoder inputs.

CONTROL LINES

The Decoder/Demultiplexers at S2 and M2 comprise the Control Lines Decoder. The select inputs S2-1,2,3 and M2-1,2,3 are connected to PR8, PR9, and PR10. $\overline{\text{R11}}$ enables S2-6 and R11 enables M2-6 (thus choosing between the two decoders); $\overline{\text{MODE CL/FF}}$ from G2-11 Decoder/Demultiplexer enables S2-5 and M2-5. The active low pulse of the selected control line is generated when clock phase $\overline{\text{Ø3}}$ enables the S2-4 and M2-4 decoder inputs.

The Disk Controller uses thirteen of the sixteen control lines.

Control line 15 cannot be used due to the structure of the micro-program instruction.

FLIP-FLOP NETWORK

The eight bit Addressable Latches (A2, S5, N1, G1, S1, A1, and B1) are multifunctional devices capable of storing single line data in eight addressable latches.

The addressable latch address inputs (pins 1, 2, and 3) are connected to PR0, PR1, and PR3, through the inverters G3-1/2, G3-3/4, and G3-5/6. PR12 determines the data to be stored; PR12=1 sets the selected flip-flop; PR12=0 resets the selected flip-flop.

The Decoder/Demultiplexer at H1 enables the selected group of eight flip-flops. R3, PR4, and PR5 select the group; $\overline{\text{PR0}}$, $\overline{\text{PR1}}$, and $\overline{\text{PR2}}$ select the flip-flop within the group.

Group selection is enabled when the controller executes a CL/FF micro-instruction. An active low signal $\overline{\text{MODE CL/FF}}$ enables H1 (H1-5 goes low). The H1 outputs, which are connected to enable pins (pin 14) of each of the flip-flop groups, generate an active low pulse on the selected output pin during the $\overline{\text{Ø3}}$ clock phase.

The groups 1, 2, 3, 4, and 5 are connected to the $\overline{\text{CCMR2}}$ signal, and a General Reset ($\overline{\text{GR}}$) signal or a Clear Controller signal clears the flip-flops in these groups. The groups 6 and 7 are connected only to the $\overline{\text{GR}}$ signal, thus the Clear Controller command does not clear these two groups of flip-flops. The Controller Flip-Flop Network includes a total of fifty-six flip-flops.

JUMP CONDITIONS NETWORK

The eight-to-one-data selector/multiplexers T1, R1, M1, H3, H7, F1, U7, E1, J1 and N2, the 2-input AND-OR invert gate M5, the OR gate K3-1,2,3, the two inverters H2-5/6 and T3-11/10 and the flip-flop at H5 make up the Jump Condition Network.

There are nine groups of jump conditions. PR10, PR11, and PR12 select the Jump Condition within one of the nine jump condition groups. The bits PR10, PR11, and PR12 are inverted by H2-9/8, H2-11/10, H2-13/12 and connected to input pins 11, 10, and 9 of T1, R1, M1, H3, H7, F1, U7, and E1 (jump condition groups 1 to 8) and J1 (group 9).

The jump condition groups 1 to 8 strobe inputs are constantly enabled via a connection to ground. The jump conditions Group 9 is enabled by an active low signal at K3-3 (PR15 OR-ed with $\overline{\emptyset 3}$).

The PROM bits PR13, PR14 and PR9 select the Jump Condition group. The strobe to this selector (N2-7) comes from K3-3 when the controller executes a jump instruction (PR15 is low). OR gate K3-1,2/3 provides this strobe signal with $\overline{\emptyset 3}$ pulse. The flip-flop JGRP9 (G1-11) controls the selecting of jump condition. When the flip-flop is reset, the controller is set, the micro-program selects the jump conditions in group 9 (J1). H2-5/6 inverter and M5-13,1,9,10/8 gate provide this selection. The state of the S/R flip-flop at H5 depends on the state of the selected jump condition.

Also this S/R flip-flop at H5 is set by a $\overline{\text{PCD}}$ (L2-7) active low pulse, whenever the PC is the destination register for an inter-register instruction. The flip-flop output (H5-4) is inverted by T3-11/10 and provides the $\overline{\text{Load PC}}$ pulse for the Program Counter. The Program Counter will be loaded with the ALU-out data and the data selected by the Multiplexer at A4; thus executing a micro program jump.

The $\overline{\text{Load PC}}$ signal is active during the time interval from the leading edge of clock phase $\overline{\emptyset 3}$ to the leading edge of the next $\overline{\emptyset 2}$ clock phase ($\overline{\emptyset 2}$ resets the S/R flip-flop at H5).

The controller includes a total of seventy-two jump conditions.

INPUTS FROM DEVICE

All input signals from device are active low.

TABLE 5-1. INPUTS FROM DEVICE

Signal Name	Pin Number	Termination Type	Receiver Location	Jump Condition Name & Location
INDEX	93	220/330 ohms	U8-1/2	Index (R1-2)
SECTOR	98	220/330 ohms	U8-9/8	Sector (U7-13)
FAULT	25	220/330 ohms	E9-9/8	DSKERR (F1-3)
UNIT	22	220/330 ohms	H9-5/6	UNRDY (H7-2)
ON CYLINDER	24	220/330 ohms	H9-3/4	ONCYL (H7-3)
WRITE PROTECTED	16	220/330 ohms	H9-9/8	DKWTPT (H7-15)
SEEK COMPL 4	298	470 ohms	U9-13/12	SKCMP3 (U7-14)
SEEK COMPL 3	97	470 ohms	U0-11/10	SKCMP2 (U7-15)
SEEK COMPL 2	96	470 ohms	U9-5/6	SKCMP1 (U7-2)
SEEK COMPL 1	95	470 ohms	U9-3/4	SKCMP0 (U7-3)
SEEK ERR	92	470 ohms	T9-9/8	SEEKER (T1-13)
READ DATA	89	100 ohms	T9-1/2	
READ CLOCK	90	100 ohms	T9-5/6	

OUTPUTS TO DEVICE

The output signals are enabled only when the controller has the device bus, i.e., the flip-flop ONBUSFF (A1-9) is set.

All output signals to device, except Terminator Monitor and Terminator Power are active low.

TABLE 5-2. OUTPUTS TO DEVICE

Signal Name	Origin	Driver Location	Pin Number
TERM POW	(+5V)	S7A-6,7/5	2
TERM MONITOR	(+5V through 150 ohms)	S7A-6,7/5	86
TRK OFFS	Flip-flop TRKOFS	A8A-1,2/3 Driver	5
EG + WG	EGWG	M9B-6,7/5	Pin 250
C.A. STRB	CASTRB	A8B-1,2/3	Pin 50
RTZS	Flip-flop RTZS	S7A-1,2/3 Driver	Pin 82
H.S. 1	Flip-flop HS1	S8A-6,7/5	88
H.S. 2	Flip-flop HS2	S6B-6,7/5	85
READ GATE	Flip-flop RDGATE	S7B-6,7/5	87
U.S. 1	Flip-flop USØ	A9A-1,2/3	4
U.S. 2	Flip-flop US1	A9A-6,7/5	9
U.S. 3	Flip-flop US2	A9B-1,2/3	3
U.S. 4	Flip-flop US3	A9B-6,7/5	10
WRITE DATA	(see Write Data Transmitter)		
C.A. 2^0	Flip-flop CABITO	A8A-6,7/5	7
C.A. 2^1	WC B7-3	C8A-1,2/3	11
C.A. 2^2	WC B7-2	C9A-6,7/5	17
C.A. 2^3	WC B7-6	C9A-1,2/3	13
C.A. 2^4	WC B7-7	C8A-6,7/5	19
C.A. 2^5	WC B6-3	C9B-6,7/5	15
C.A. 2^6	WC B6-2	C9B-1,2/3	14
C.A. 2^7	WC B6-6	C8B-1,2/3	12
C.A. 2^8	WC B6-7	C8B-6,7/5	18

NOTE: The gate S6B-6,7/5 is wired-OR with the gate S6A-6,7/5. With the jumper JM removed, S6A-7 is low and the output at pin 85 is $\overline{\text{H.S.2}}$.

UNIT PROTECT AND SINGLE DENSITY JUMPERS

The unit is protected whenever the respective protect jumper is inserted.

The Unit Protect (UP0-UP3) jumpers are located at P1 and are connected to the 4-input multiplexer at P2. The inverted output P2-14 is connected to jump condition UNTPRT (F1-14).

A removed jumper indicates a non-protected unit.

If the Disk Unit is single density, the respective Single Density jumper must be inserted. The Single Density (SD0-SD3) jumpers are located at P1 and connected to the 4-input multiplexer at P2. The inverted output, P2-2 is connected to jump condition SNGNDJC (J1-15). A removed jumper indicates a Double Density Disk.

MAINTENANCE SWITCHES

The LS switch is the ON-OFF Line Switch and is connected to jump condition ONOFLN. In the "ON" position, the switch permits normal controller activity. In the "OFF" position, the switch disconnects the controller from the AQ bus of the computer and places the controller in the Maintenance mode. In this mode, the AND gate input U4-13 will be low as will the U4-12 input. The sequencer input U6-4 will also be low thus disabling sequencer operation. Consequently, all A/Q commands received will generate an internal reject.

The type of operation performed is now a function of the positions of the maintenance switches (MS1-MS4).

MS1 is connected to jump condition MSW1 (J1-14).

MS2 is connected to jump condition MSW2 (J1-2).

The OFF-line operation initiated on the first disk which is ready conforms to the following table.

TABLE 5-3. OFF-LINE OPERATION

MS2	MS1	Operation
OFF	OFF	Seek Cylinder 5
OFF	ON	Seek Cylinder 73
ON	OFF	Seek Cylinder 10
ON	ON	Seek Cylinder 146

JUMPER JM

NOTE 1: The Mode jumper (JM) determines the activity mode of the EX-OR gates at R4. When the JM jumper is inserted, T3-2 is high and the gates listed above invert the data transferred by the receivers (T9). For a removed JM jumper, the gates transfer the data without inversion.

MAINTENANCE PHILOSOPHY

Maintenance philosophy for the CDDC is to use diagnostics requiring minimal operator intervention through the operators panel to determine that the controller is defective.

The defective module should be replaced in the field and taken to a depot for repair.

OPERATING ADJUSTMENTS

No operating adjustments are required, except for the initial setting of the manual control jumpers.

PREVENTIVE MAINTENANCE

Preventive Maintenance is limited to running diagnostics.

VOLTAGE MARGINS

The CDDC can operate with a ±5% voltage variation from nominal voltages.

ENVIRONMENTAL

NON-OPERATING ENVIRONMENT

The CDDC can withstand a temperature range from -30°F to +150°F (-35°C to +65°C), and a maximum thermal shock not to exceed 20°F/hour (2.2°C) with no permanent effect on operating characteristics.

OPERATING ENVIRONMENT

The CDDC can operate at a temperature range from 40°F to 120°F (4.4°C to 43.3°C), withstand a maximum thermal shock of 0.2°F per minute, and a relative humidity range from 10 to 90 percent.

TABLE 6-1. AQ/DMA PIN ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	+5VDC	52	+12VDC -**	201	+5VDC	252	DMA-MPE/
2	+5VDC TERM POWER	53	DMA-MAB01/	202	+5VDC	253	DMA-MAB11/
3	U.S.3/	54	DMA-MAB02/	203	SD01/	254	DMA-MAB12/
4	U.S.1/	55	DMA-MAB03/	204	RD01/	255	DMA-MAB13/
5	TRK OFFS./	56	DMA-MAB04/	205	SD02/	256	DMA-MAB14/
6	GND	57	DMA-MAB05/	206	RD02/	257	DMA-MAB15/
7	C.A. 2^0	58	DMA-MAB06/	207	SD03/	258	(DMA-MAB16/)
8	NA*	59	DMA-MAB07/	208	RD03/	259	DMA-MCTM/**
9	U.S.2/	60	DMA-MAB08/	209	SD04/	260	DMAx-MR/
10	U.S.4/	61	DMA-MAB09/	210	RD04/	261	DMAxRA/
11	C.A.2^1/	62	DMA-MAB10/	211	SD05/	262	DMA-MDS/
12	C.A.2^7/	63	DMA-WRITE	212	ADR05/	263	DMA-MAE/
13	C.A.2^3/	64	DMA-DTM01/	213	RTERM/**	264	DFM01
14	C.A.2^6/	65	DMA-DTM02/	214	RD05/	265	DFM02
15	C.A.2^5/	66	DMA-DTM03/	215	SD06/	266	DFM03
16	WRITE PROTECTED	67	DMA-DTM04/	216	REPLY/	267	DFM04
17	C.A.2^2/	68	DMA-DTM05/	217	ADR06/	268	DFM05
18	C.A.2^8/	69	DMA-DTM06/	218	RD06/	269	DFM06
19	C.A.2^4/	70	DMA-DTM07/	219	SD07/	270	DFM07
20	NA*	71	DMA-DTM08/	220	REJECT/	271	DFM08
21	NA*	72	DMA-DTM09/	221	RD07/	272	DFM09
22	UNIT RDY/	73	DMA-DTM10/	222	ADR07/	273	DFM10
23	NA*	74	DMA-DTM11/	223	SD08/	274	DFM11
24	ON CYLINDER/	75	DMA-DTM12/	224	RD08/	275	DFM12
25	FAULT /	76	DMA-DTM13/	225	SD09/	276	DFM13
26	GND	77	DMA-DTM14/	226	RD09/	277	DFM14
27	NA*	78	DMA-DTM15/	227	(PRIORITY)	278	DFM15
28	NA*	79	DMA-DTM16/	228	SD10/	279	DFM16
29	NA*	80	AUTOLOAD/	229	RD10/	280	ADR01/
30	NA*	81	NA*	230	SD11/	281	ADR08/
31	NA*	82	RTZS/	231	RD11/	282	ADR09/
32	GND	83	GND	232	DMA-PROT/	283	ADR10/
33	NA*	84	BUS NEED/	233	SD12/	284	ADR11/
34	NA*	85	H.S. 2^1	234	RD12	285	ADR12/
35	(DMA-MAB17/)	86	TERM MONITOR	235	SD13/	286	ADR13/
36	(DMAx MAB18/)	87	READ GATE/	236	RD13/	287	ADR14/
37	NA*	88	H.S. 2^0	237	DMA-PFLT/	288	ADR15/
38	NA*	89	READ DATA/	238	SD14/	289	ADR16/
39	SLOW-DMA	90	READ CLK/	239	RD14/	290	WRITE/
40	NA*	91	NA*	240	SD15/	291	PROG-PROT/
41	NA*	92	SEEK ERR./	241	RD15/	292	WEO/
42	NA*	93	INDEX /	242	DMA-MPB/**	293	ENPRTSYS/
43	NA*	94	NA*	243	SD16/	294	NA*
44	NA*	95	SEEK COMPL.1/	244	RD16/	295	NA*
45	DMA-MPL/	96	SEEK COMPL.2/	245	ADR04/	296	NA*
46	MR/	97	SEEK COMPL.3/	246	ADR03/	297	NA*
47	CHARINPUT/**	98	SECTOR/	247	ADR02/	298	SEEK COMPL.4/
48	STERM/**	99	BUS BUSY /	248	READ-SSTB/	299	NA*
49	WRITE DATA/	100	ALT FORCE/	249	INTRPT /	300	FORCE BUS/
50	C.A. STRB /	101	GND	250	EG+WG/	301	GND
51	-12VDC**	102	GND	251	GND	302	GND

Asterisks (*) indicate notes. See table sheet 2.

TABLE 6-1. AQ/DMA PIN ASSIGNMENT (sheet 2 of 2)

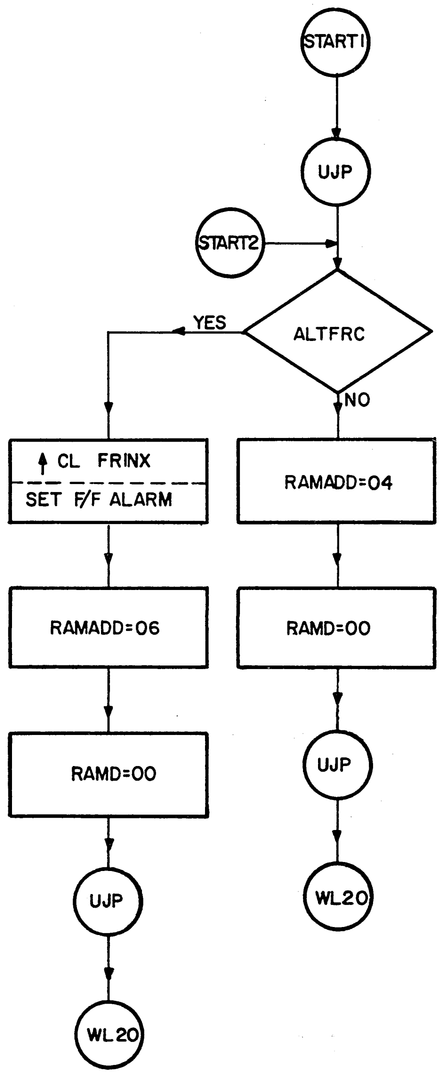
NOTES:

1. Signals marked with an asterisk (*) are not used by the CDD Controller. However, they are generated or received by the controller logic circuits. Therefore, these signal pins must be free, that is not wired.

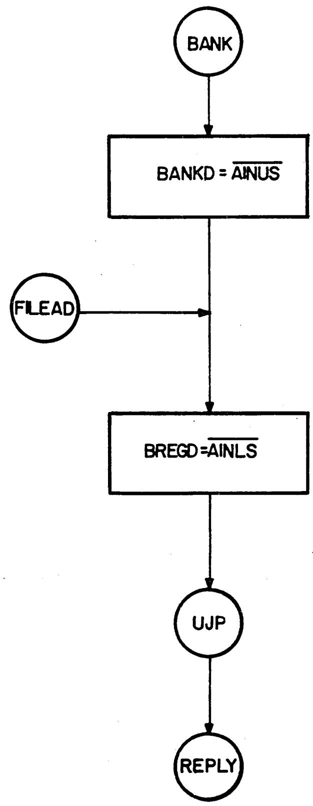
2. Pins marked with two asterisks (**) are not used by the controller. They may or may not be pre-wired on the MP backplane.

3. All signals followed by a slash (/) are active low.

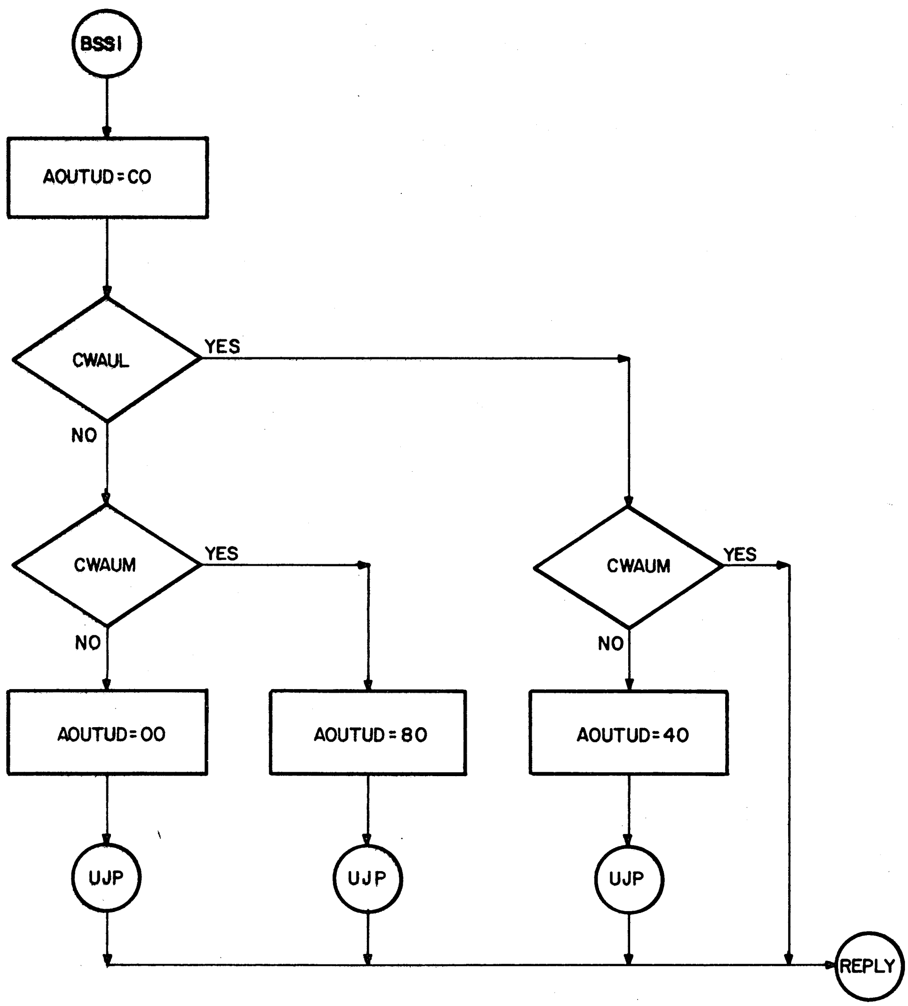
4. Unit Select and Seek Complete signals 1 through 4 correspond to units 0 through 3.



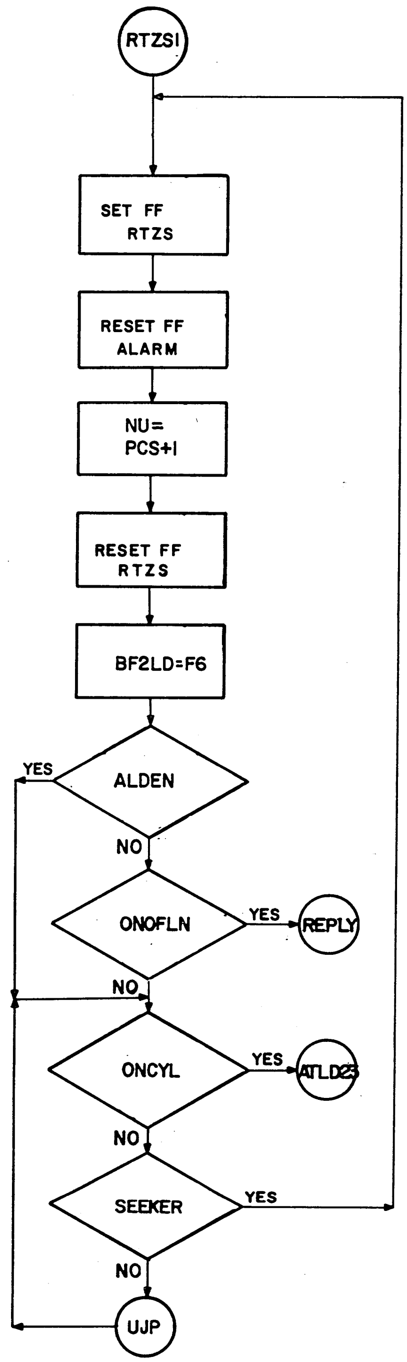
START
and
BUS RELINQUISH STATUS



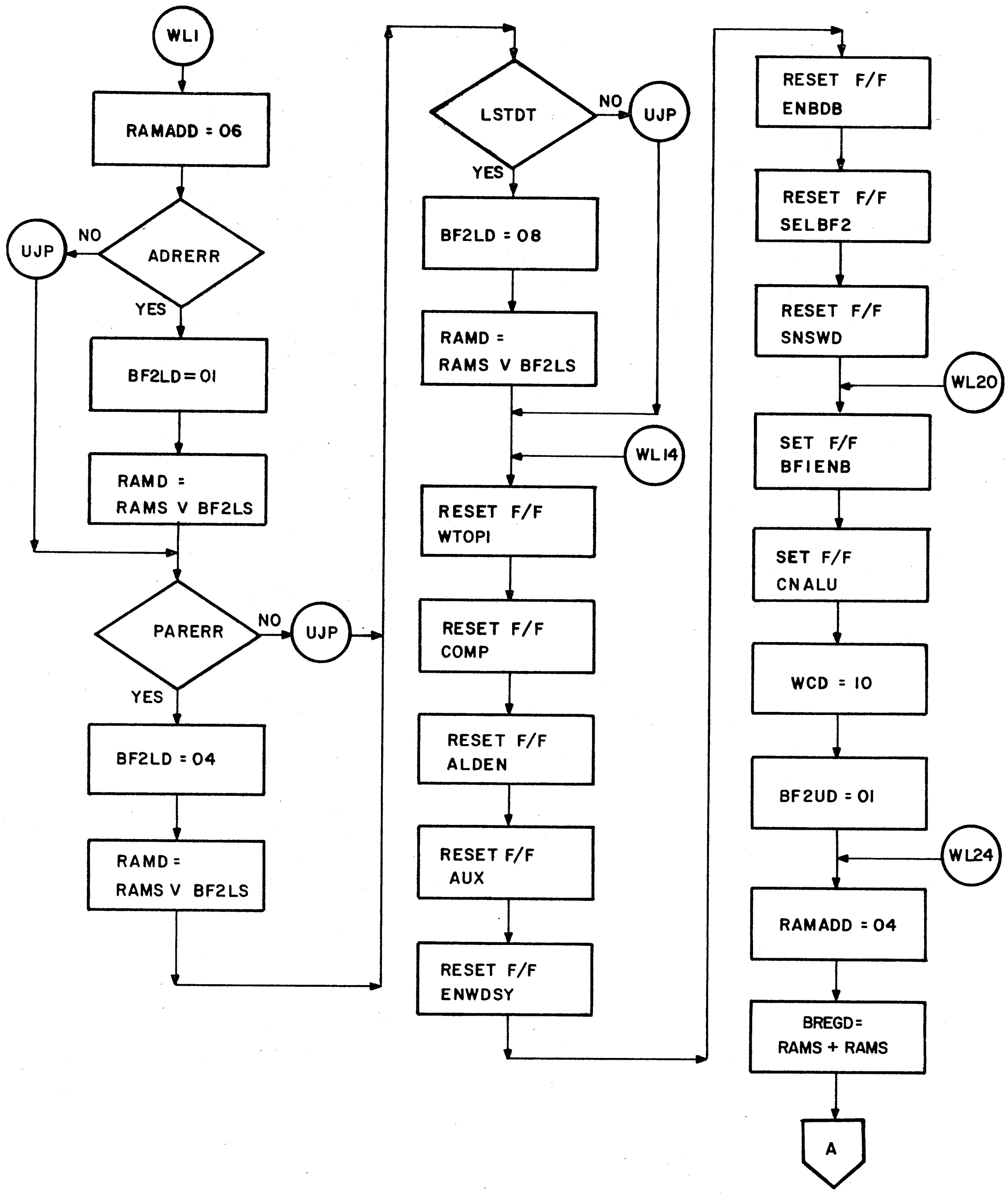
MEMORY BANK SELECT
and
LOAD FILE ADDRESS
COMMANDS



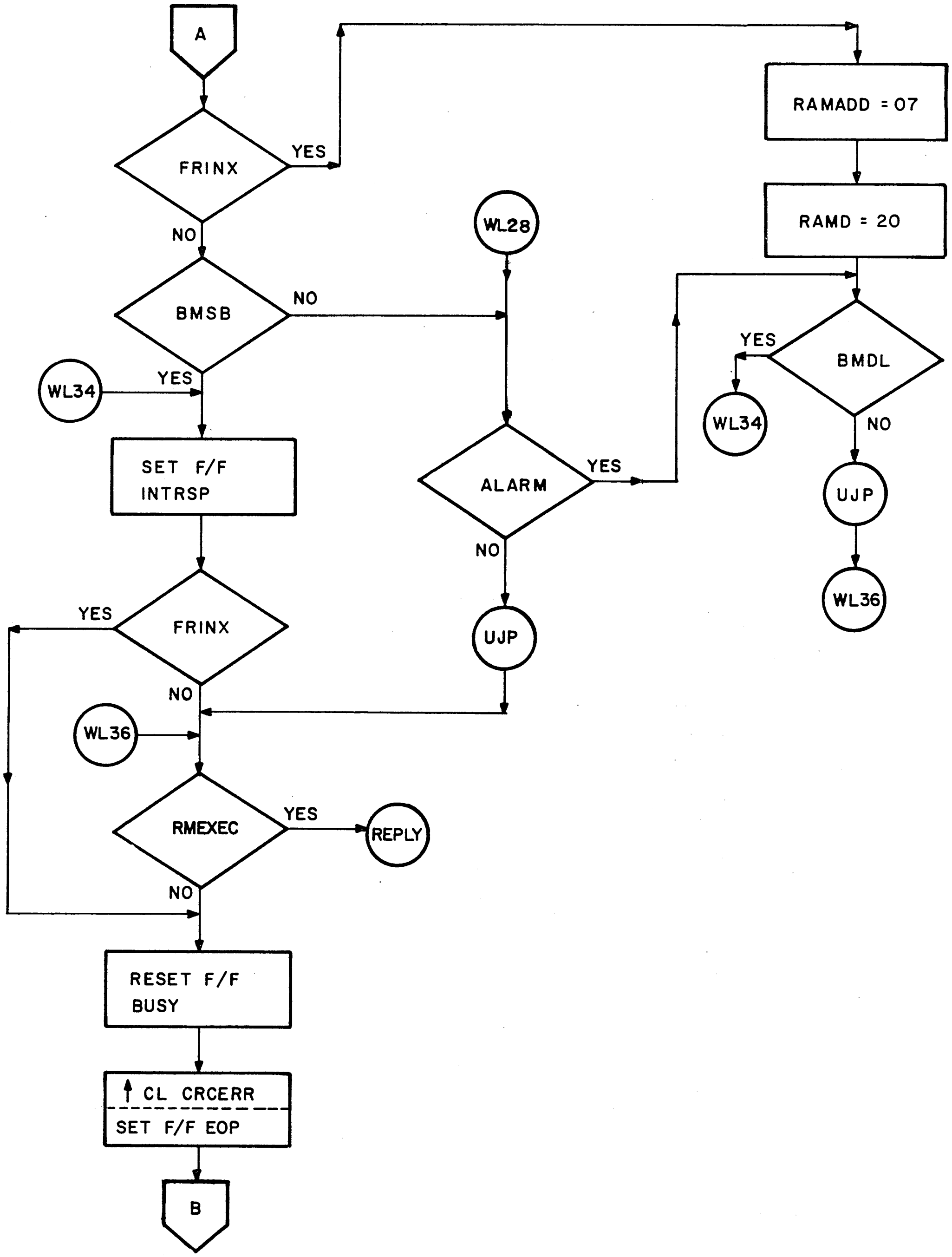
MEMORY BANK SELECT STATUS COMMAND



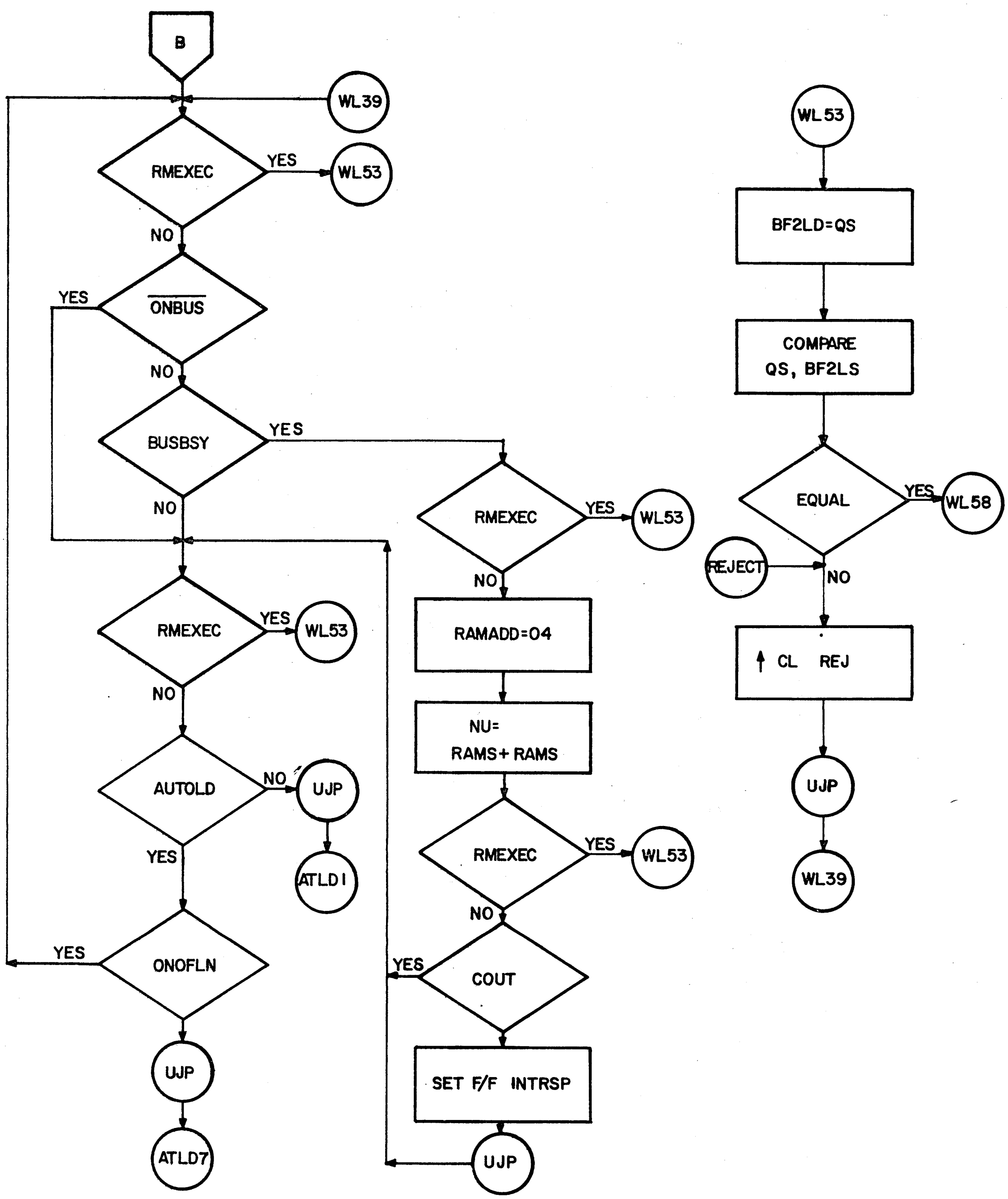
RTZS COMMAND



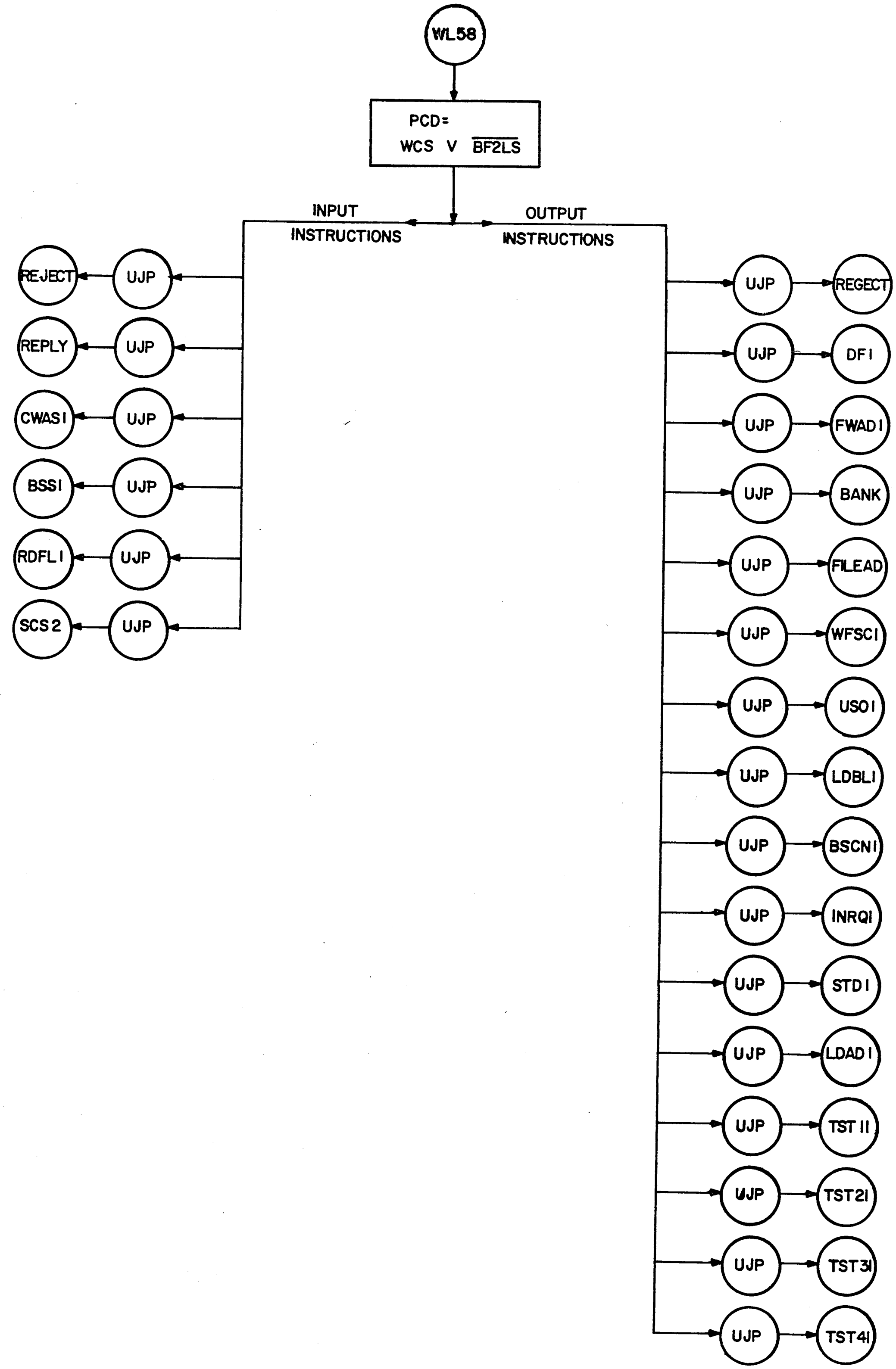
WAITING LOOP and TERMINATION OF BUSY ROUTINES



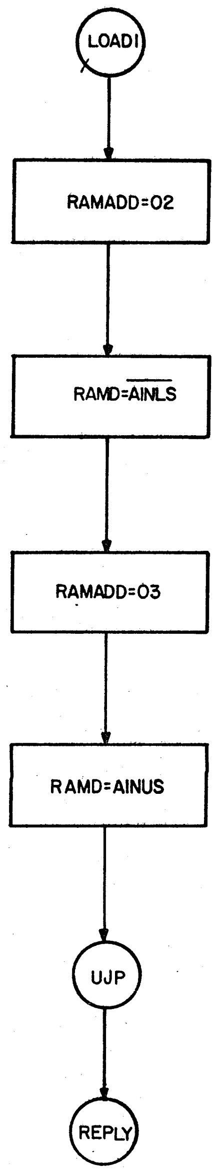
WAITING LOOP and TERMINATION OF BUSY ROUTINES (Continued)



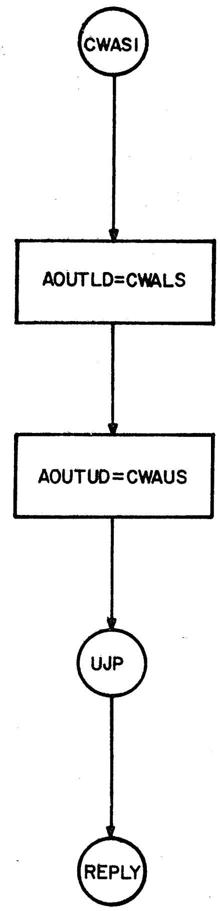
WAITING LOOP and TERMINATION OF BUSY ROUTINES (Continued)



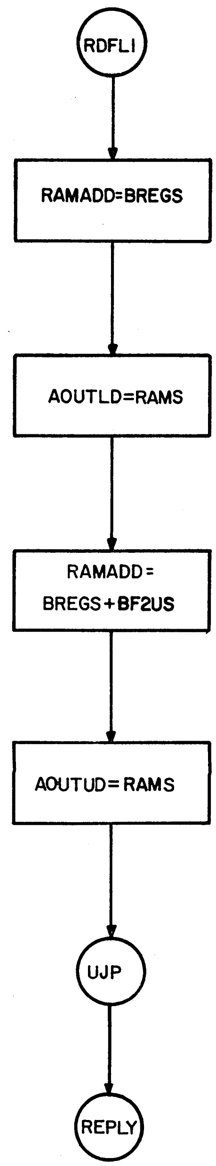
INPUT and OUTPUT INSTRUCTION DECODE



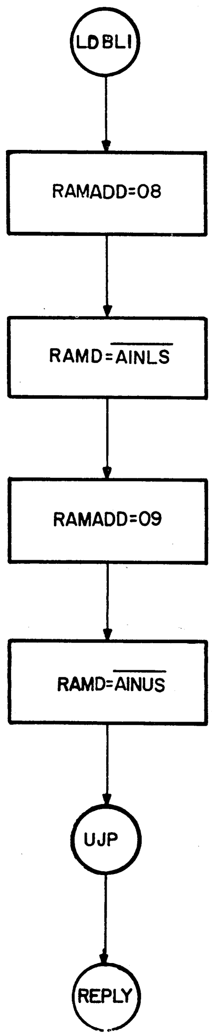
LOAD DISK ADDRESS COMMANDS



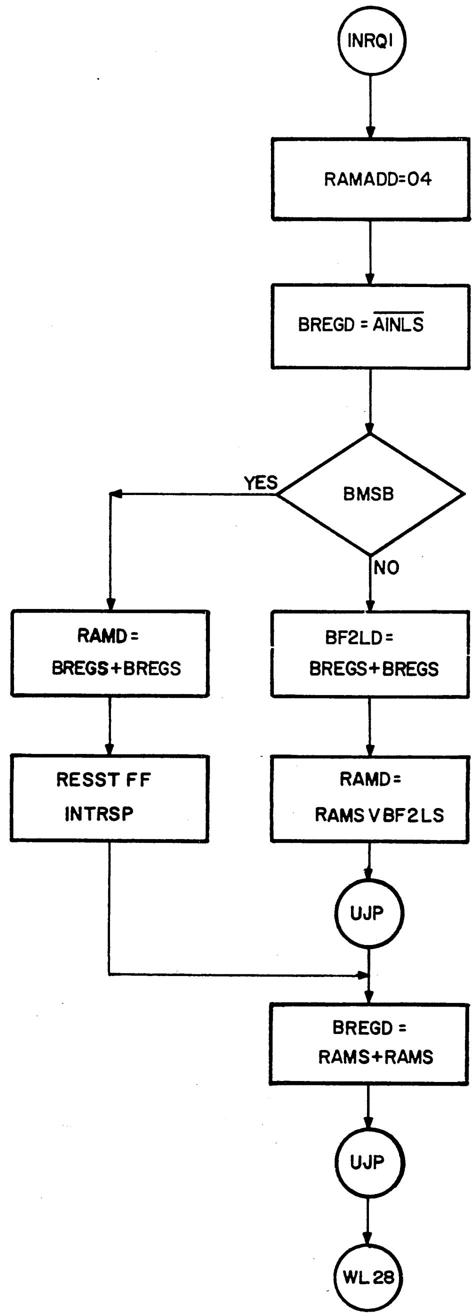
CURRENT WORD STATUS COMMAND



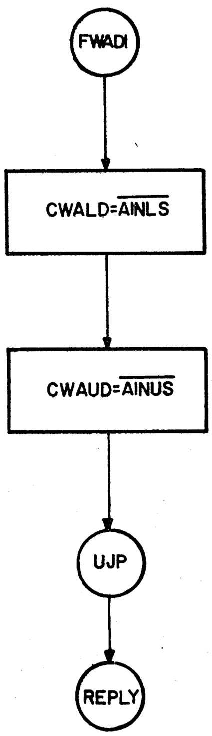
FILE STATUS COMMAND



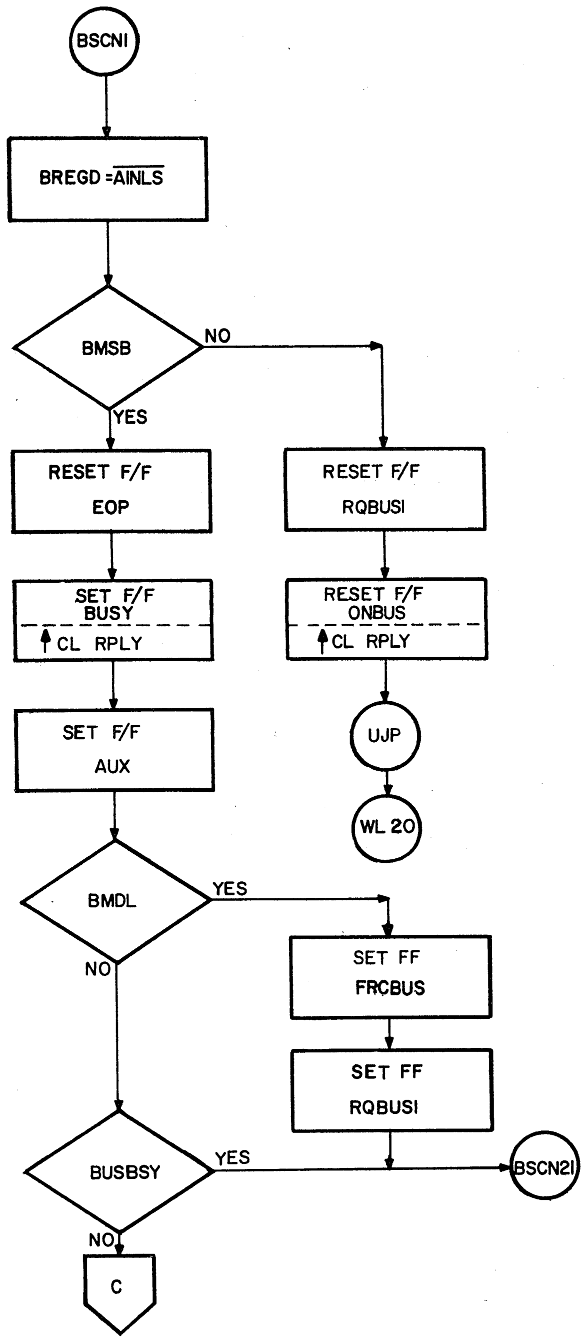
LOAD BLOCK LENGTH
COMMAND



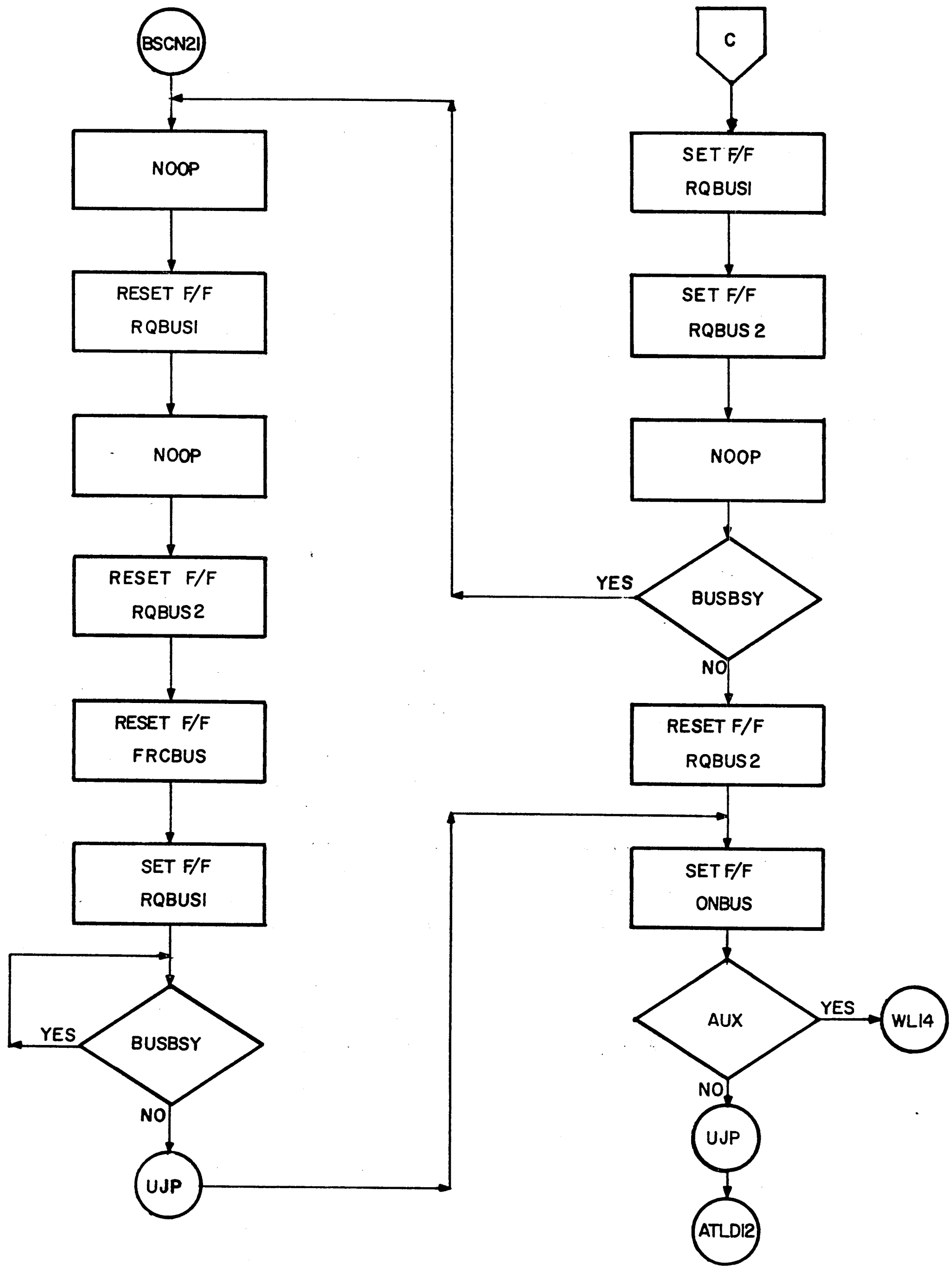
INTERRUPT REQUEST
COMMAND



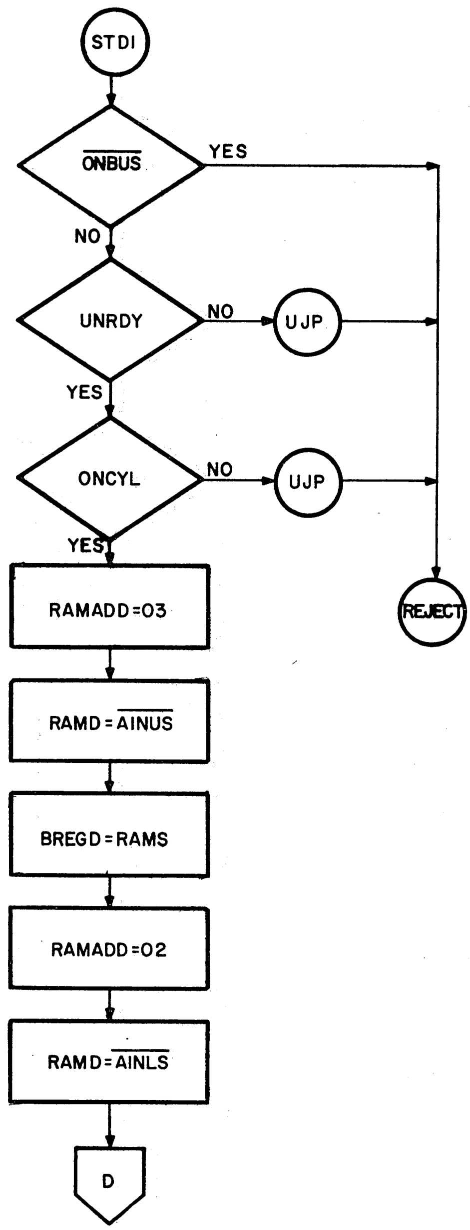
FIRST WORD ADDRESS COMMAND



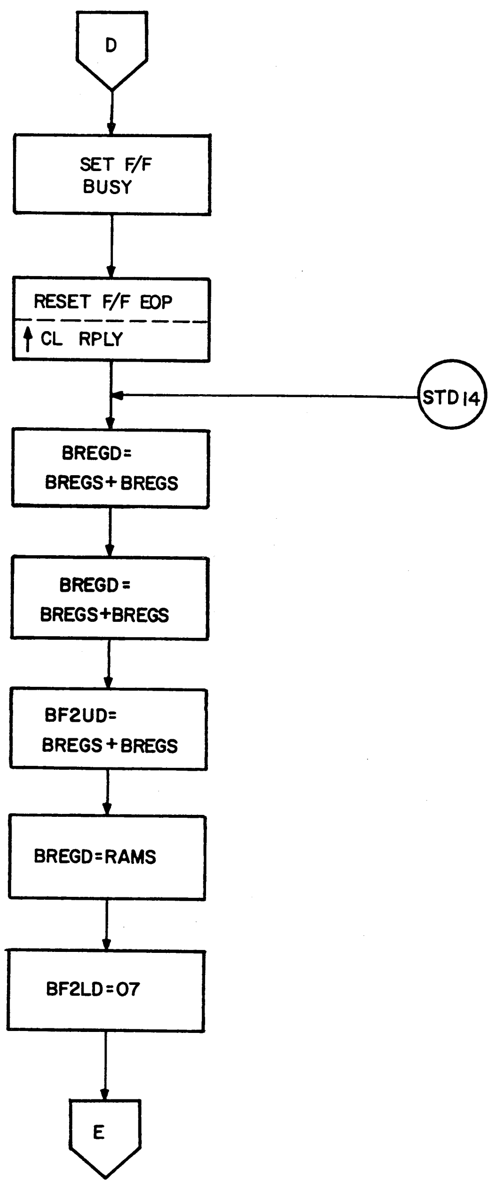
BUS CONNECT COMMAND



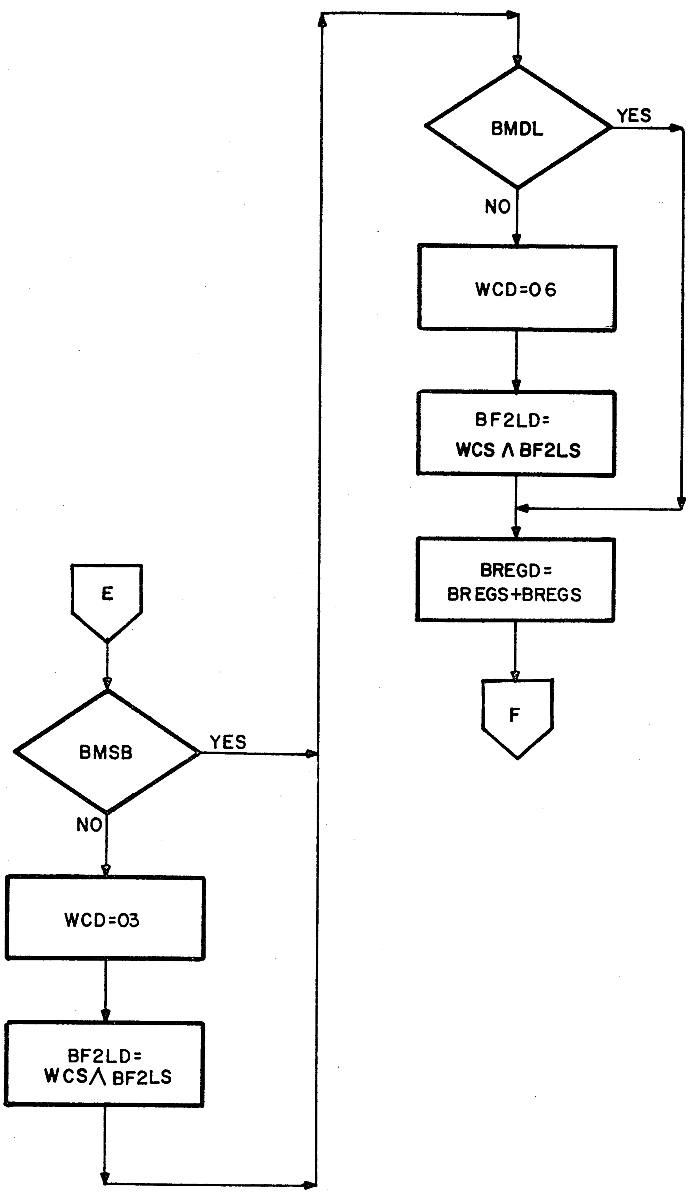
BUS CONNECT COMMAND (Continued)



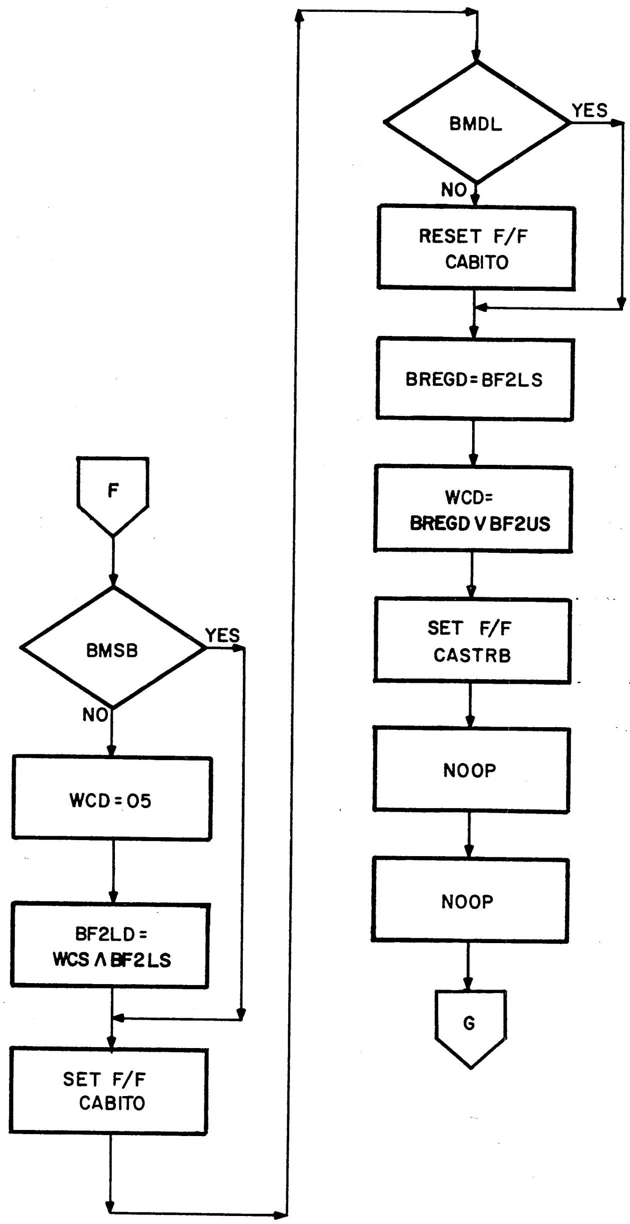
SEEK TO DEVICE
COMMAND



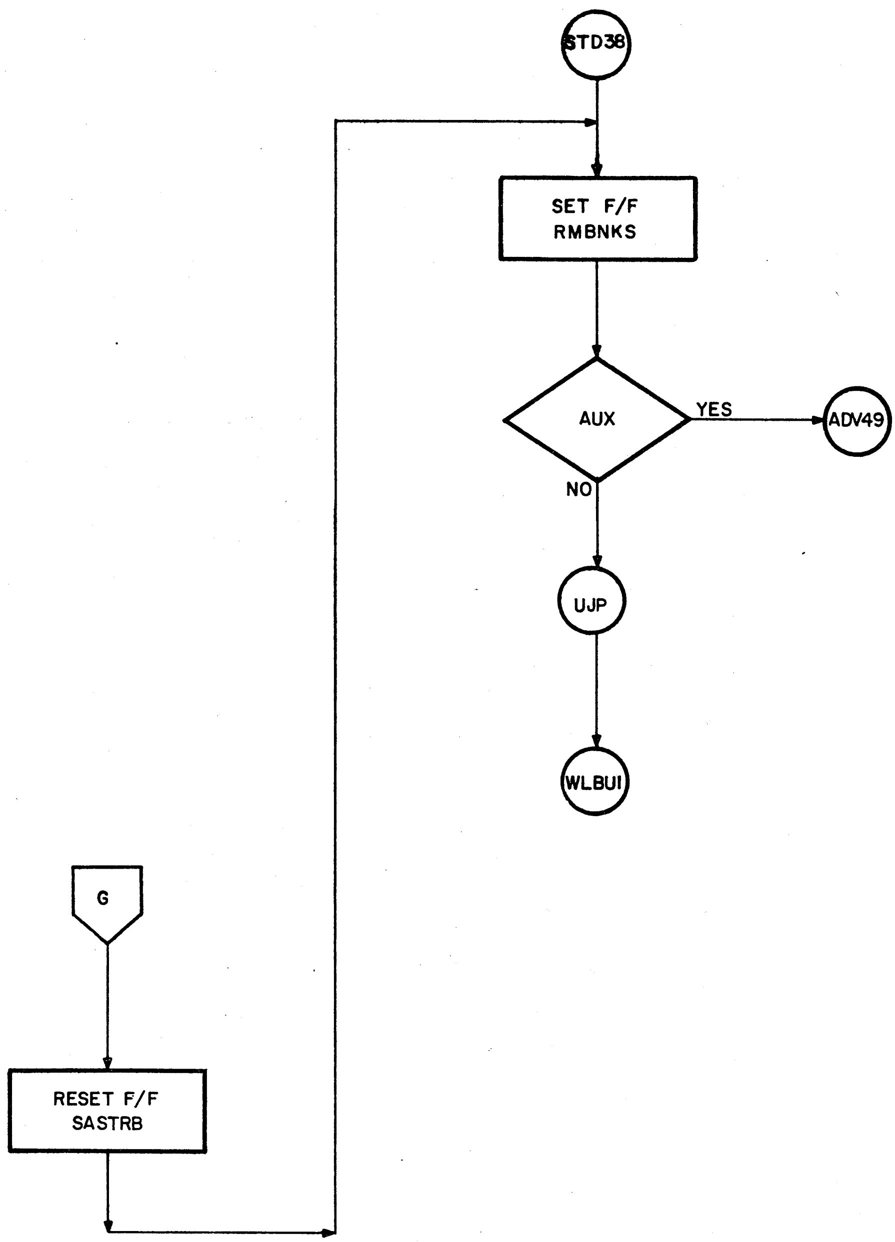
SEEK TO DEVICE COMMAND (Continued)



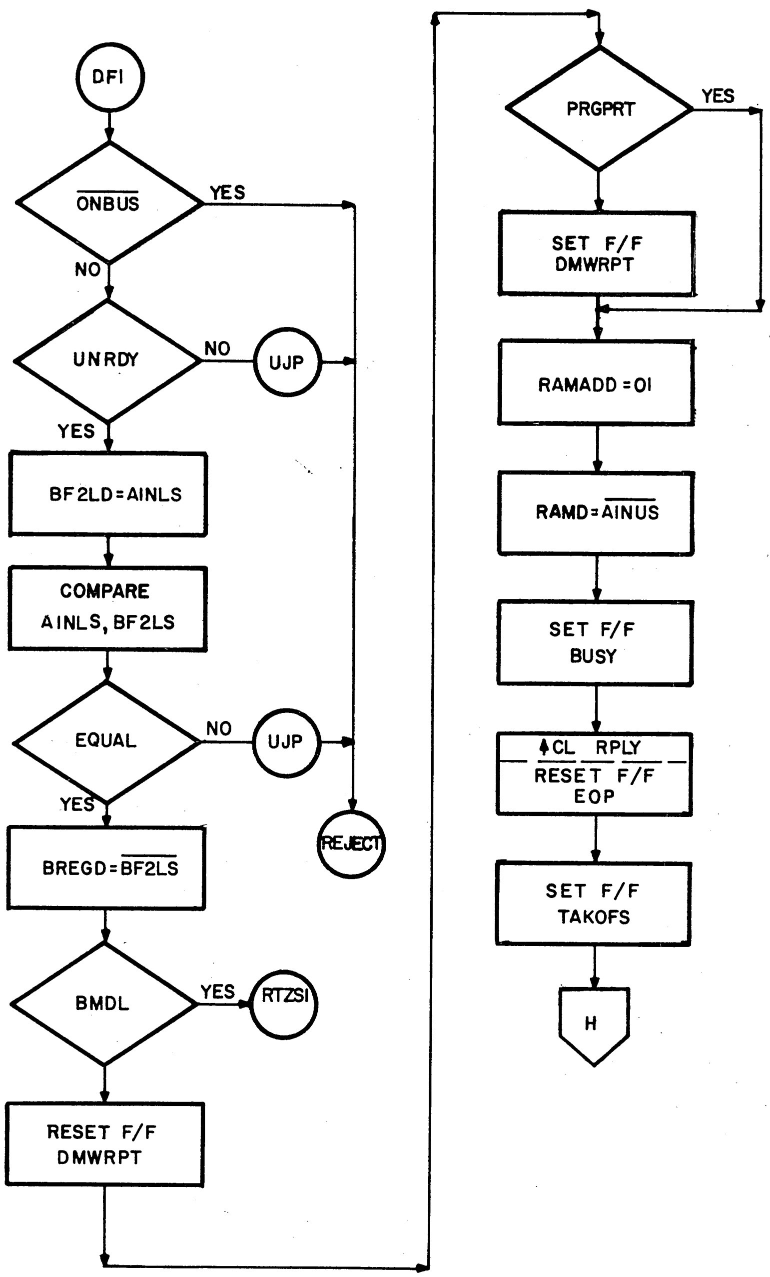
SEEK TO DEVICE COMMAND (Continued)



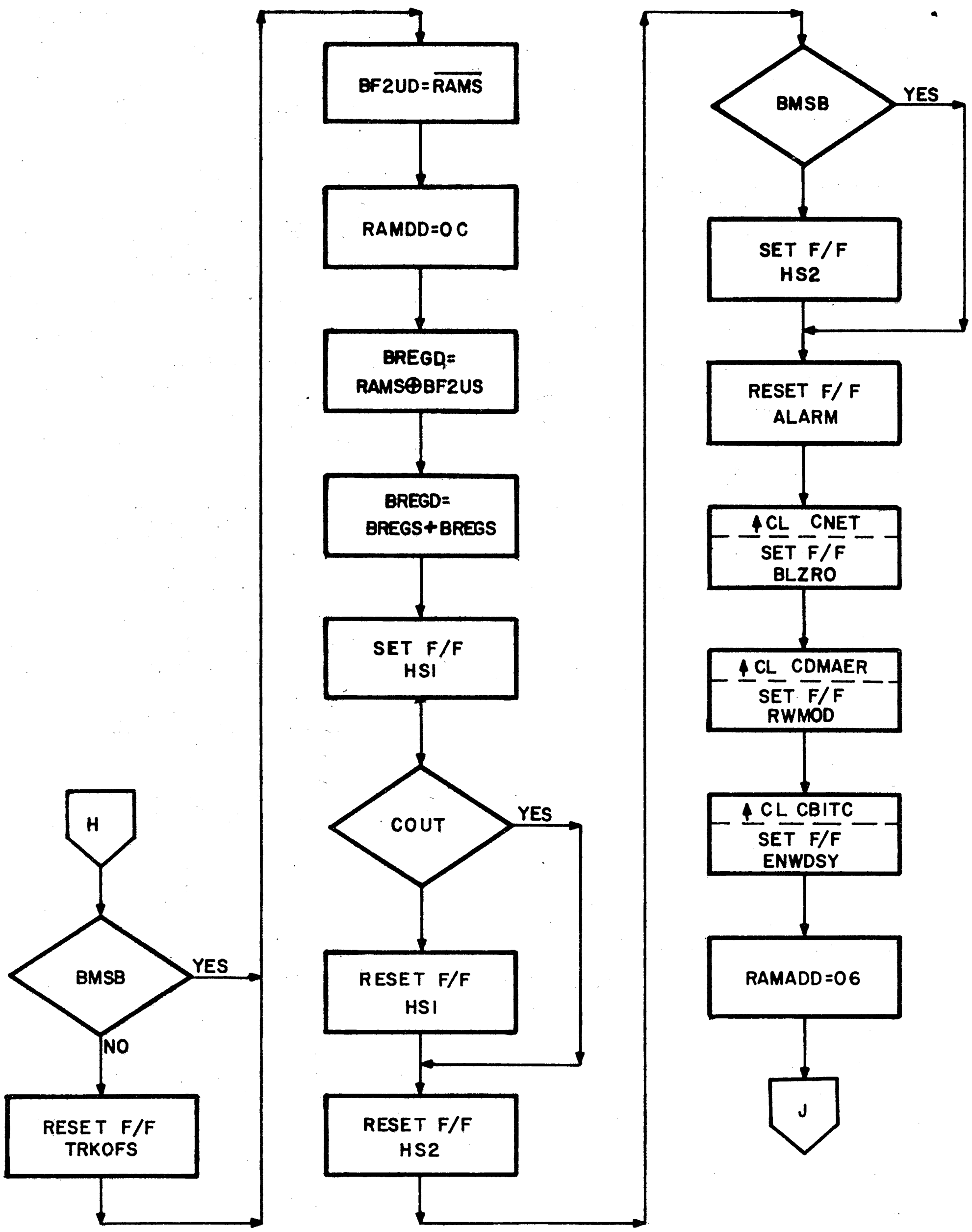
SEEK TO DEVICE COMMAND (Continued)



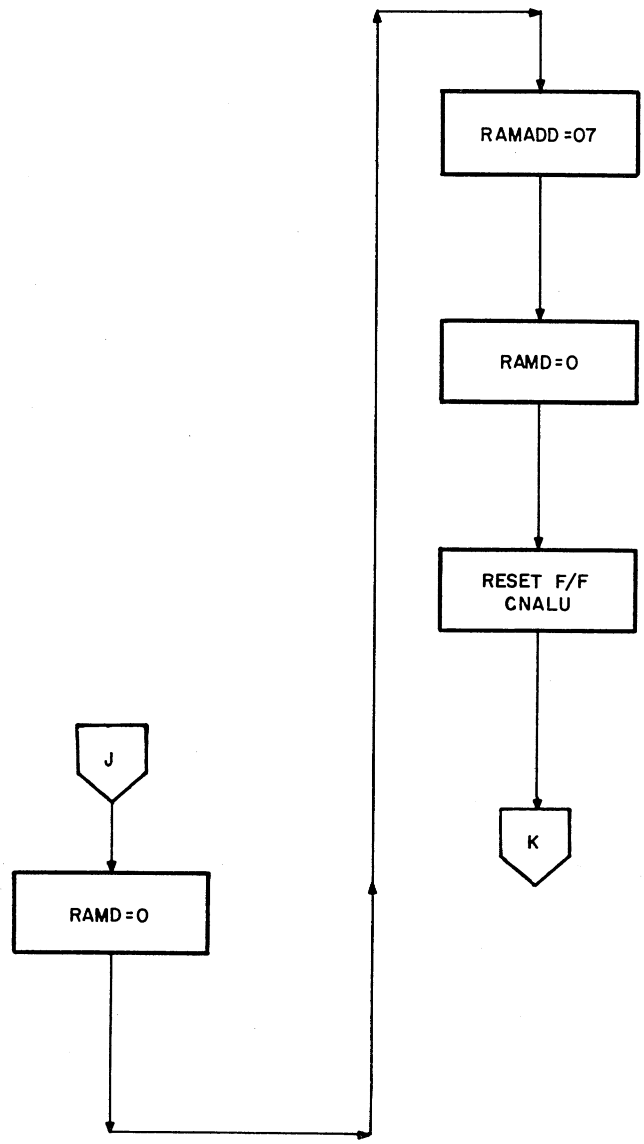
SEEK TO DEVICE COMMAND (Continued)



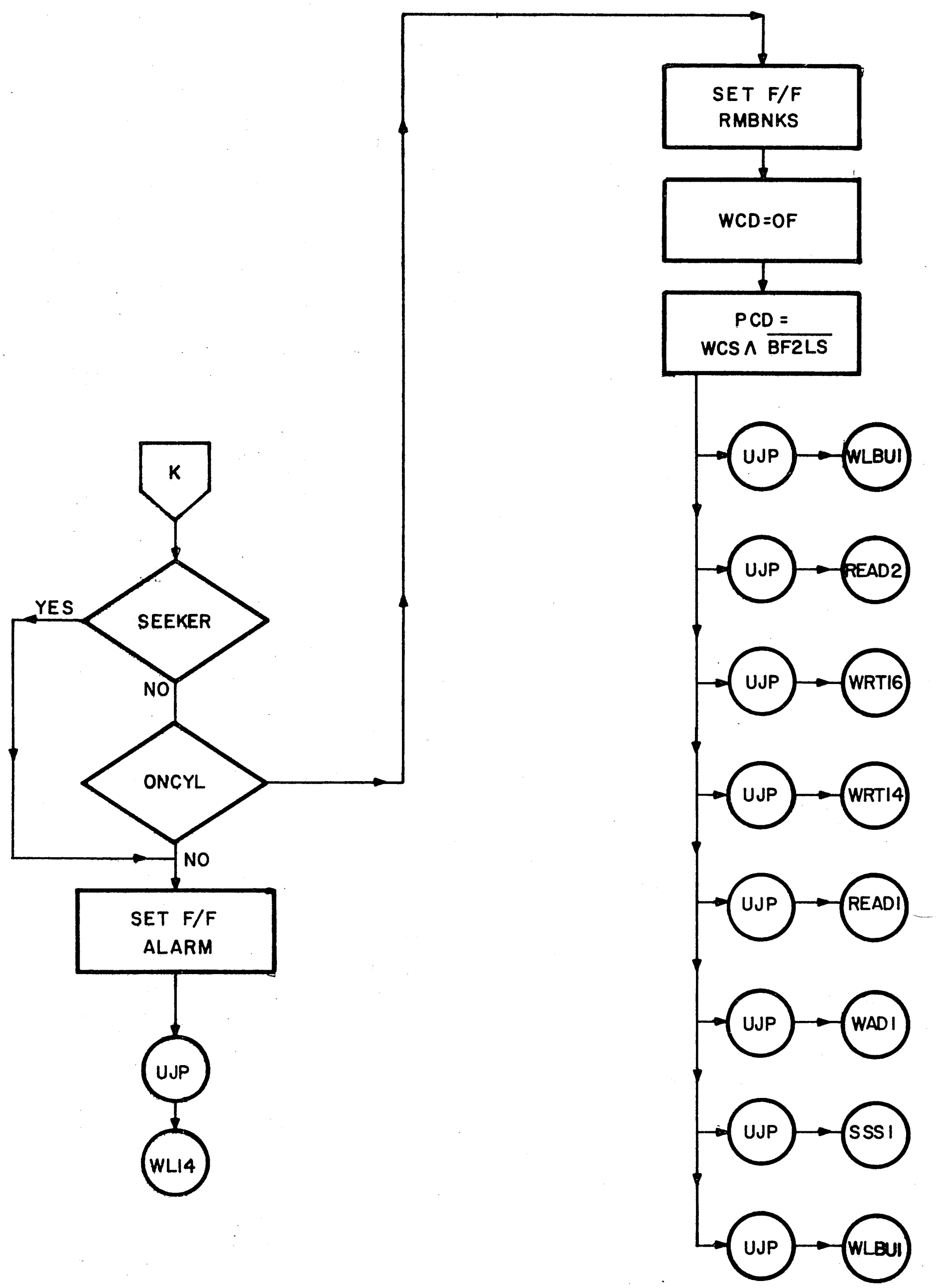
DIRECTOR FUNCTION ROUTINE



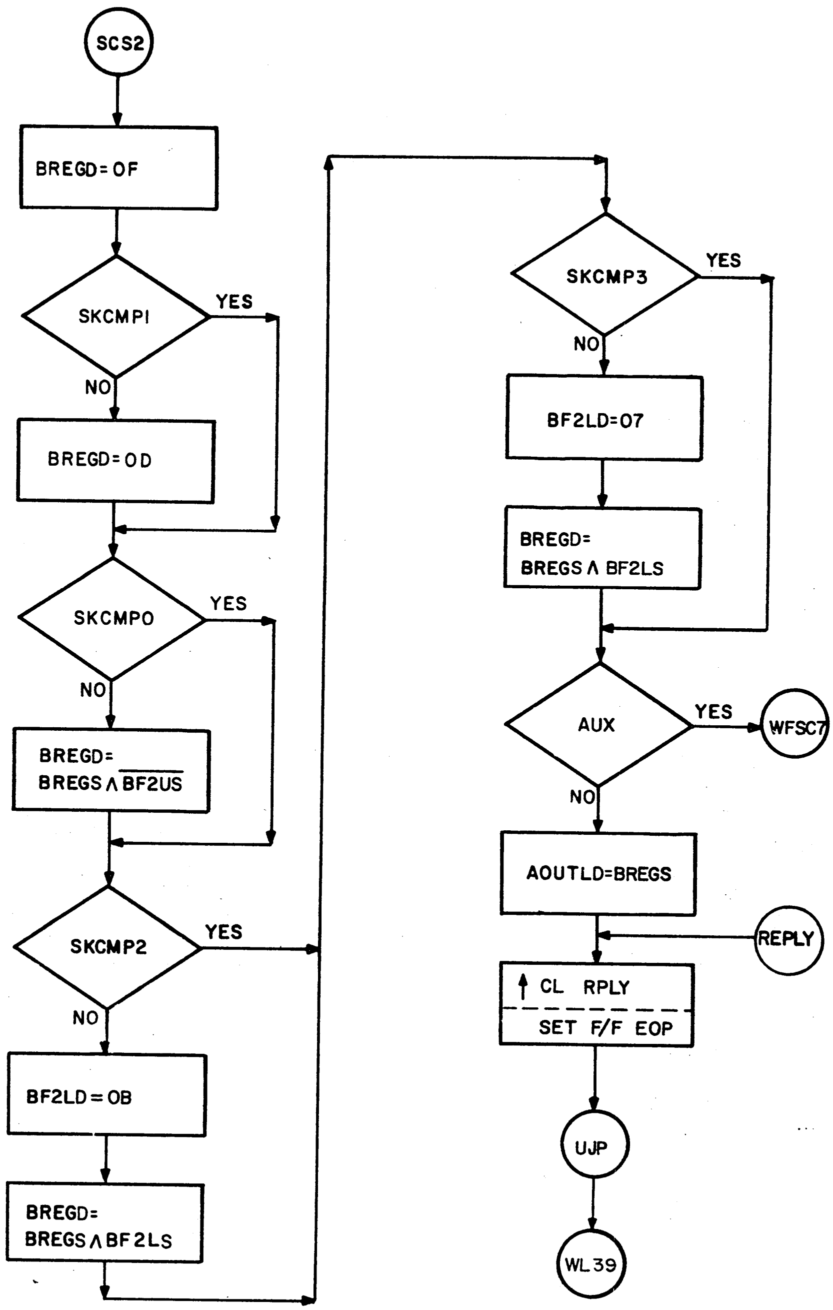
DIRECTOR FUNCTION ROUTINE (Continued)



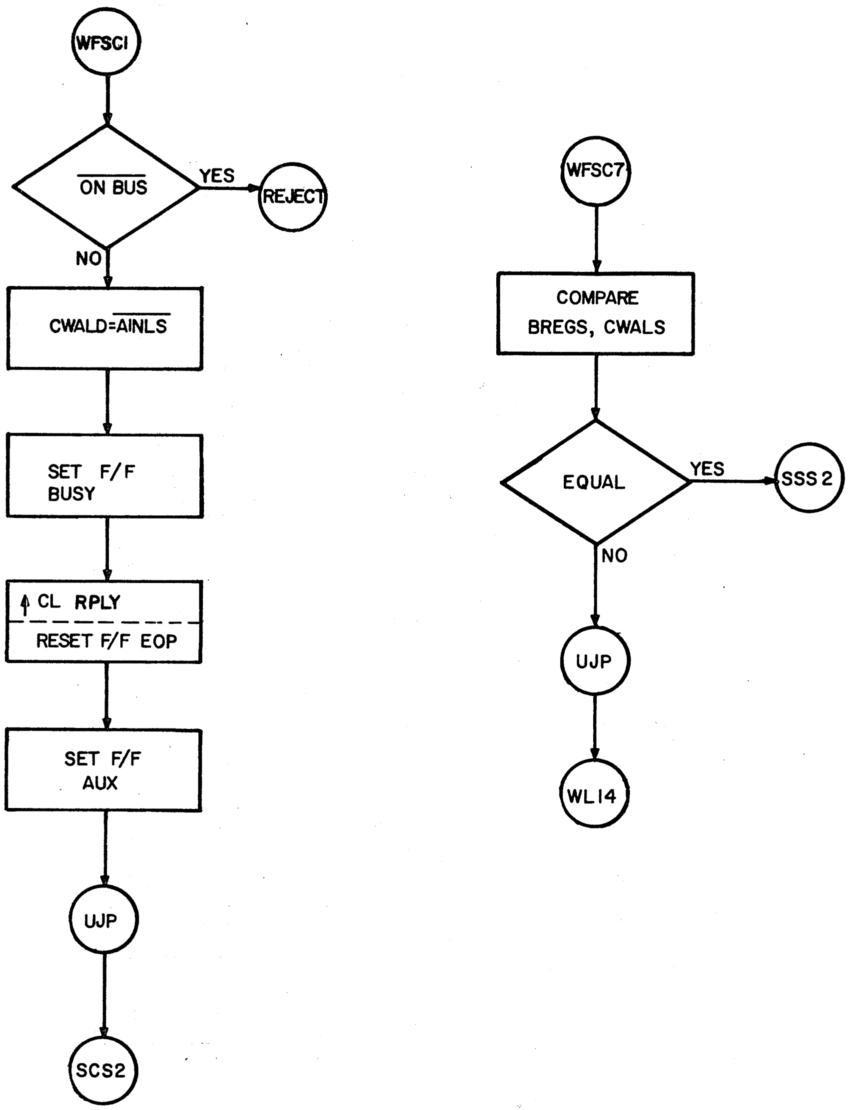
DIRECTOR FUNCTION ROUTINE (Continued)



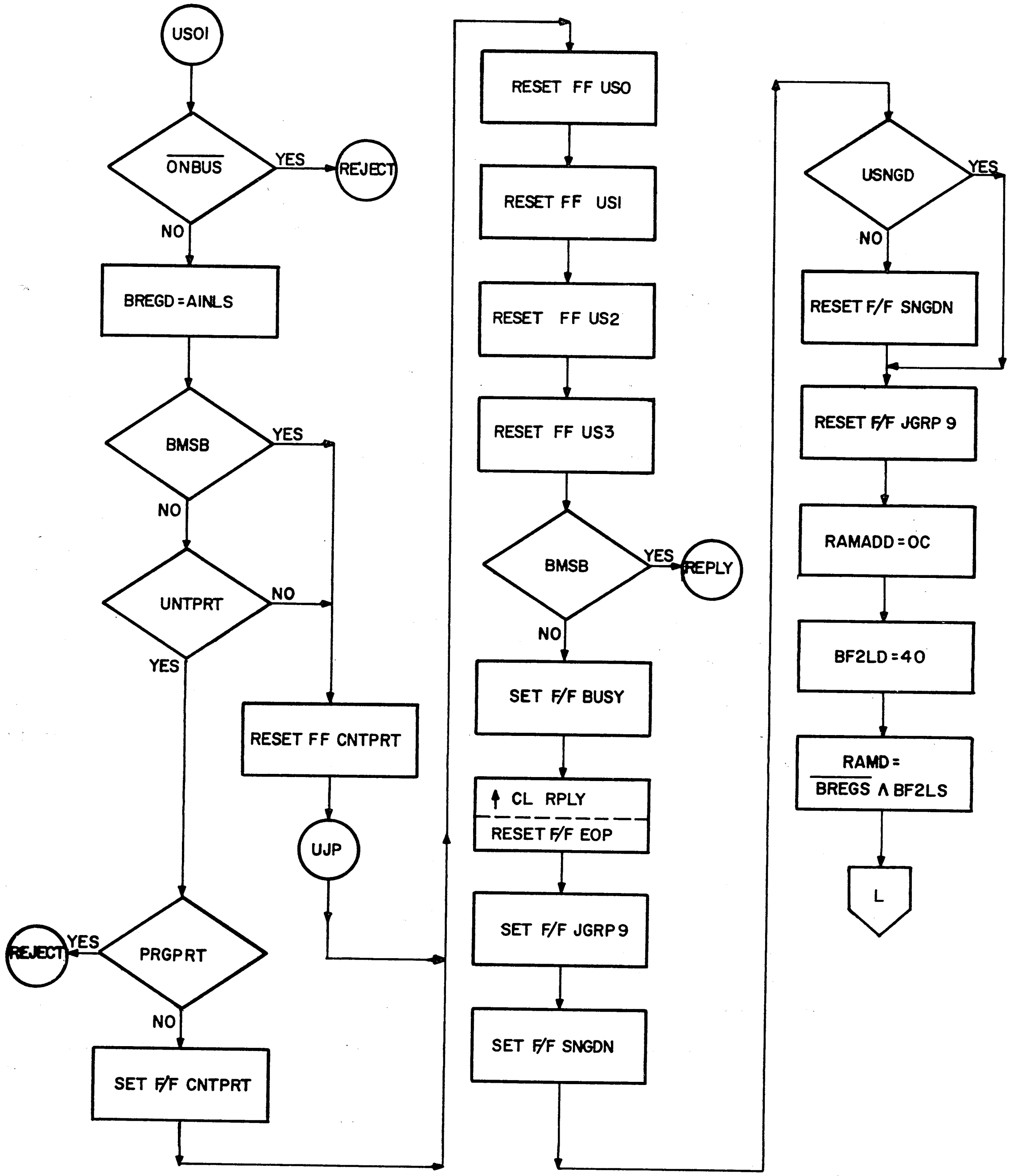
DIRECTOR FUNCTION ROUTINE (Cont'd)
and
DIRECTOR FUNCTION DECODE



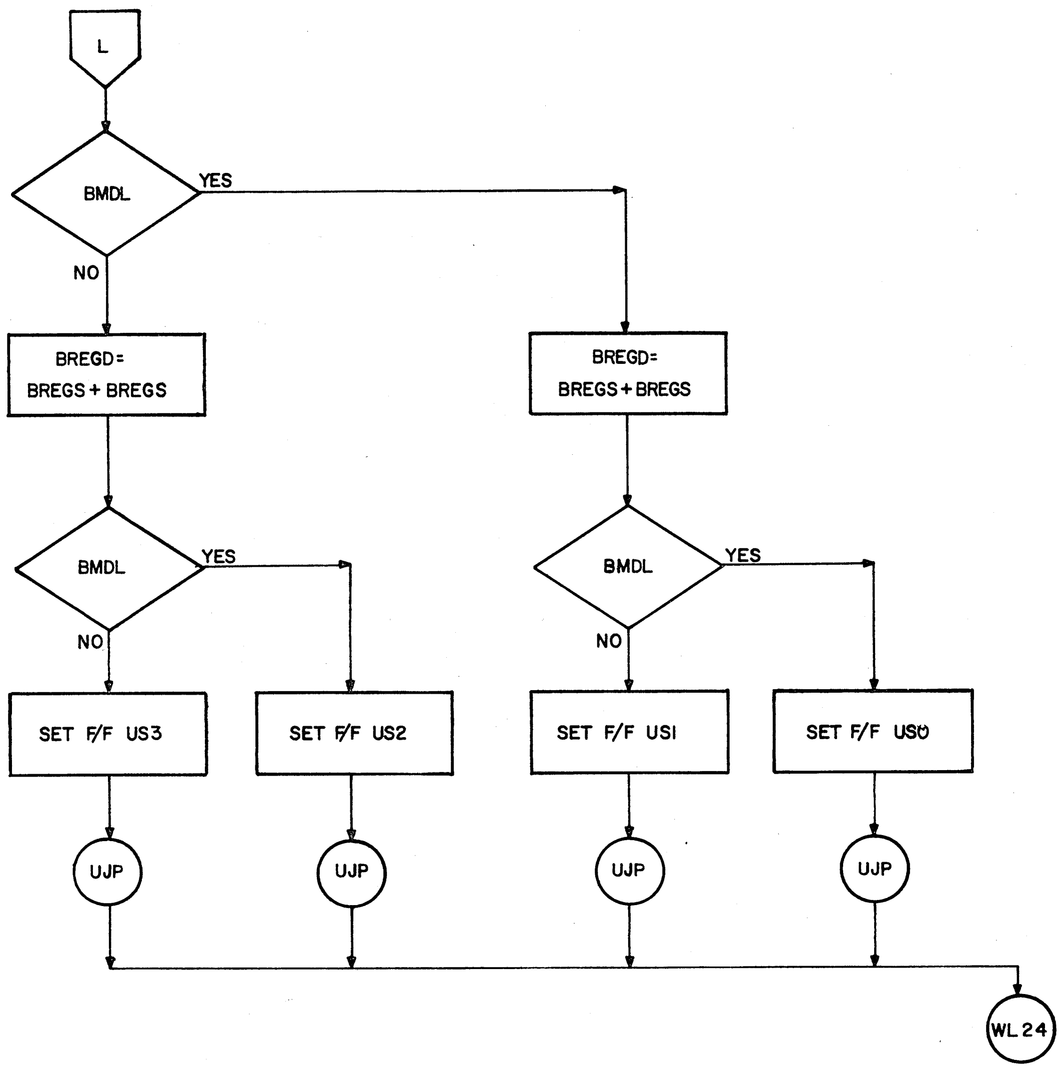
SEEK COMPLETE STATUS
COMMAND



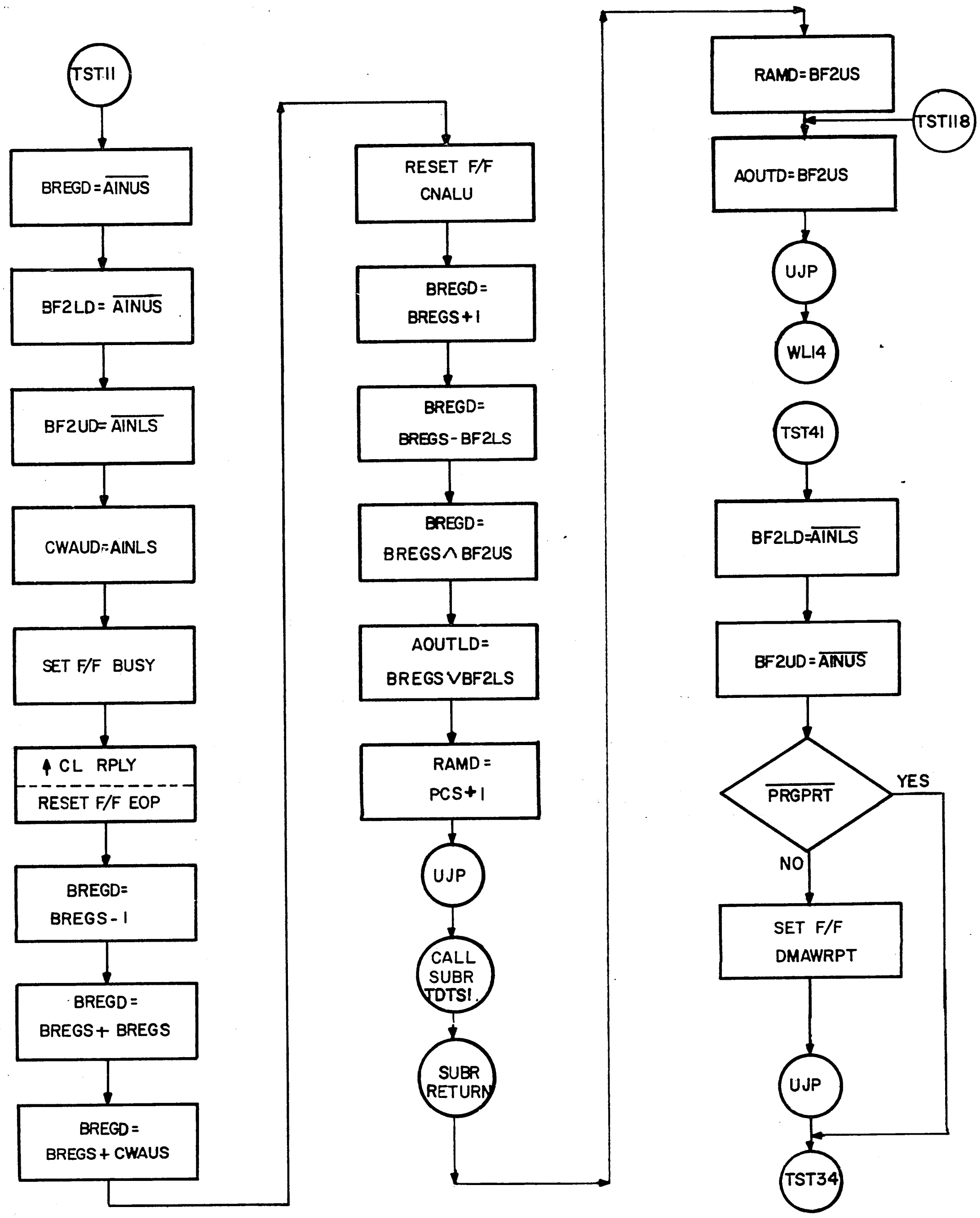
WAIT FOR SEEK CHANGE
COMMAND



UNIT SELECT
COMMAND

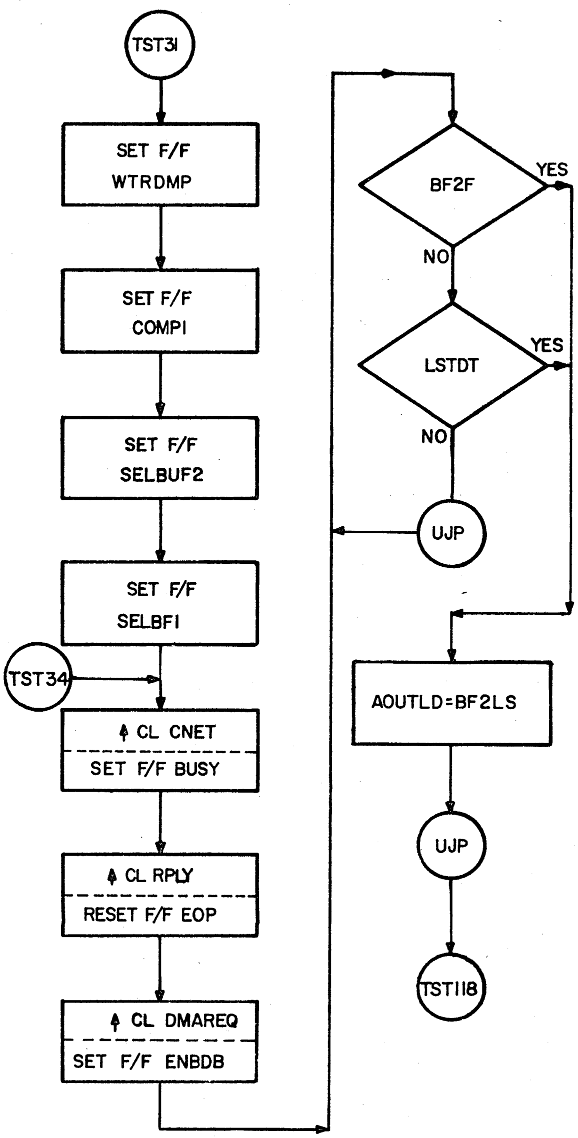


UNIT SELECT COMMAND (Continued)

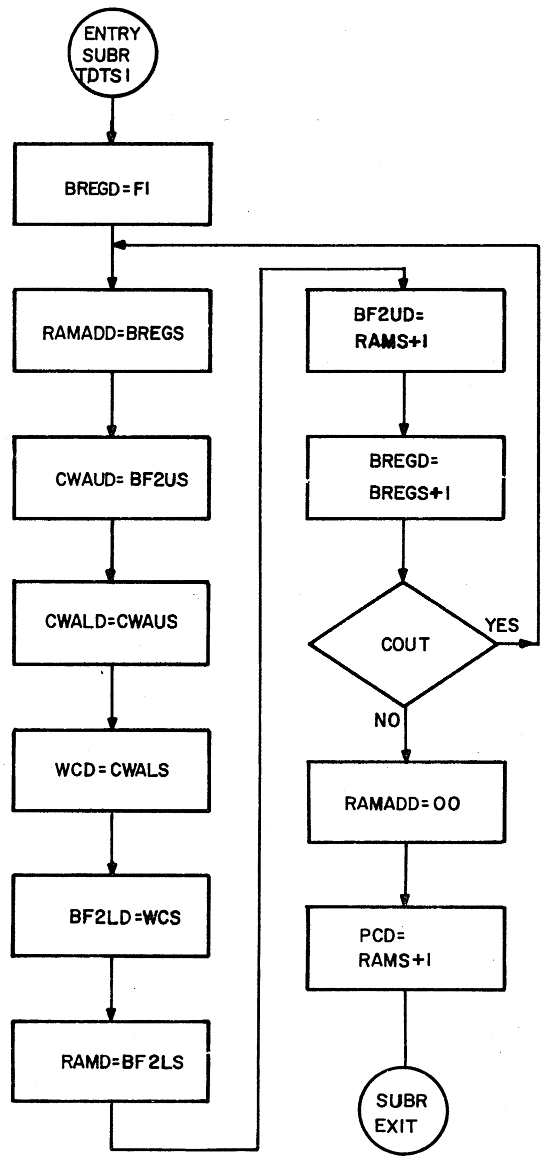


SELF TEST 1
COMMAND

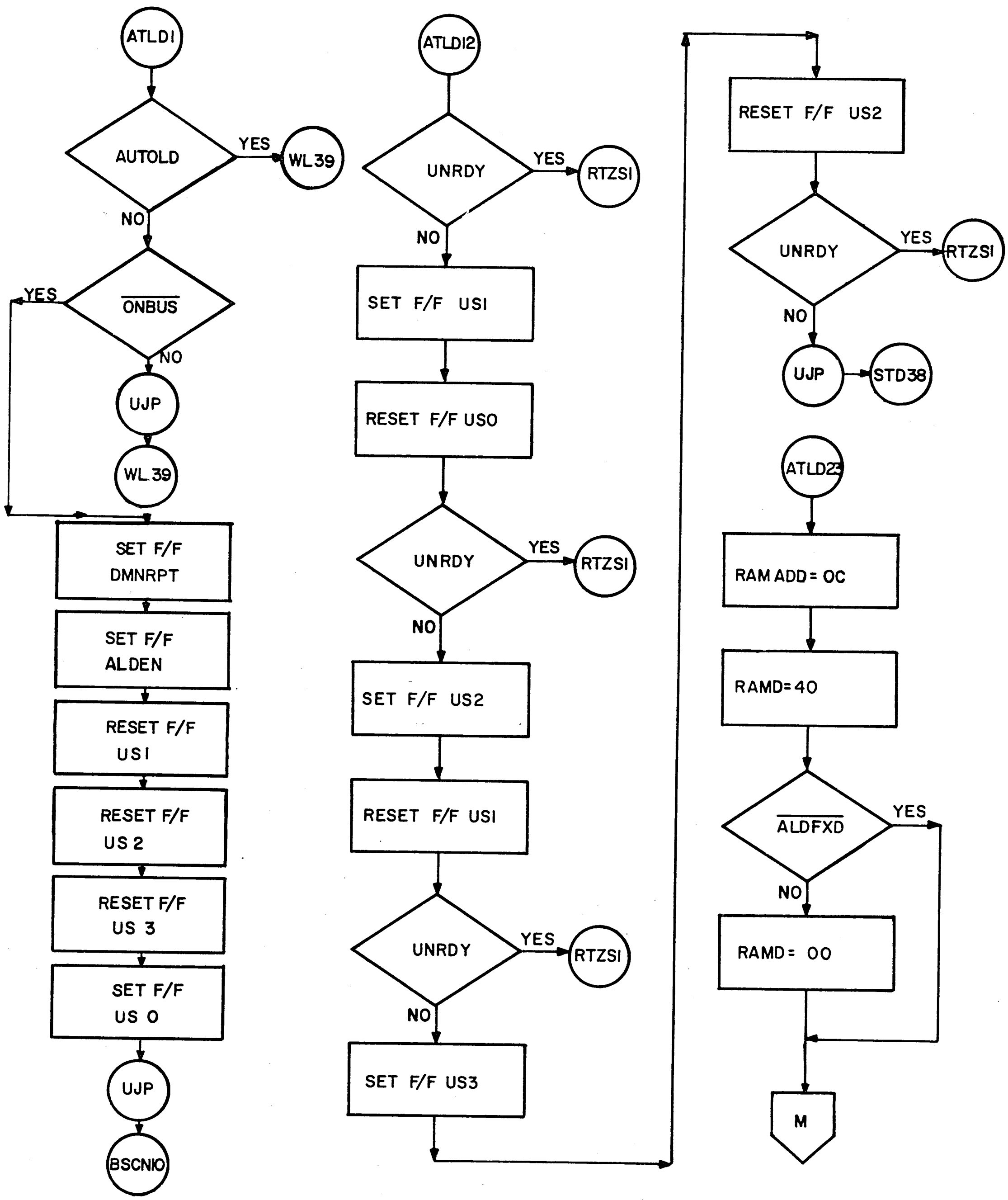
SELF TEST 4
COMMAND



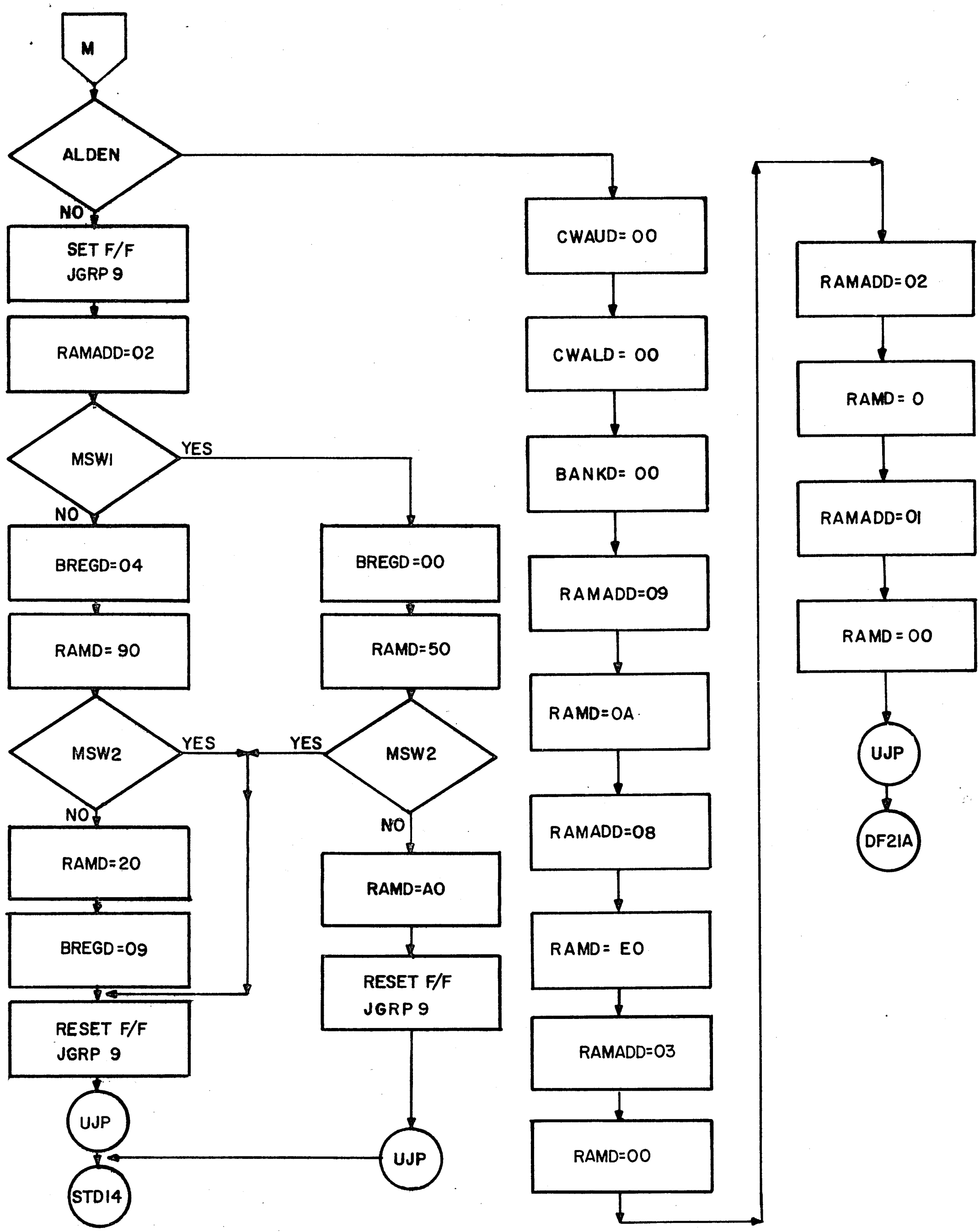
SELF TEST 3
COMMAND



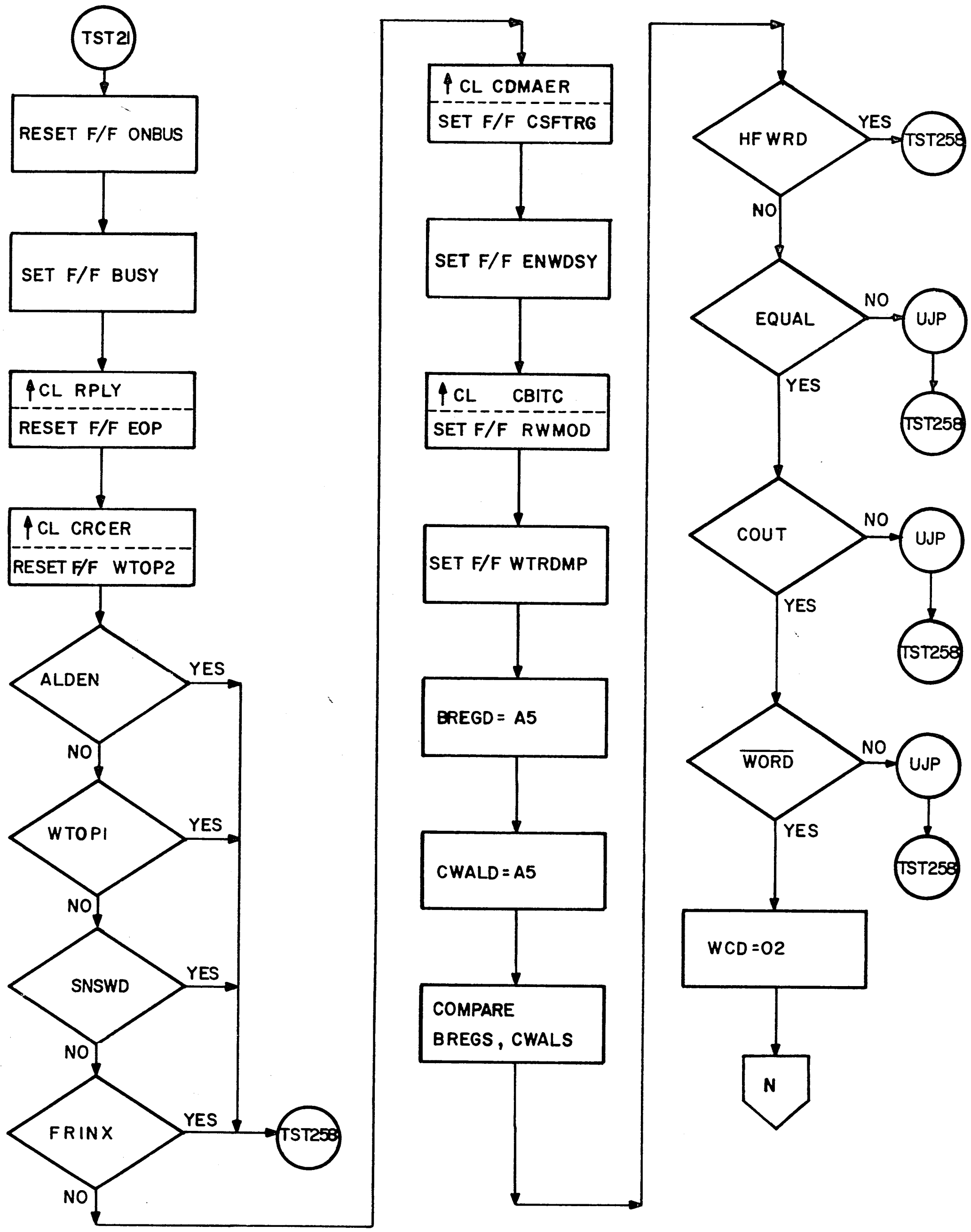
TEST 1 DATA SUBROUTINE



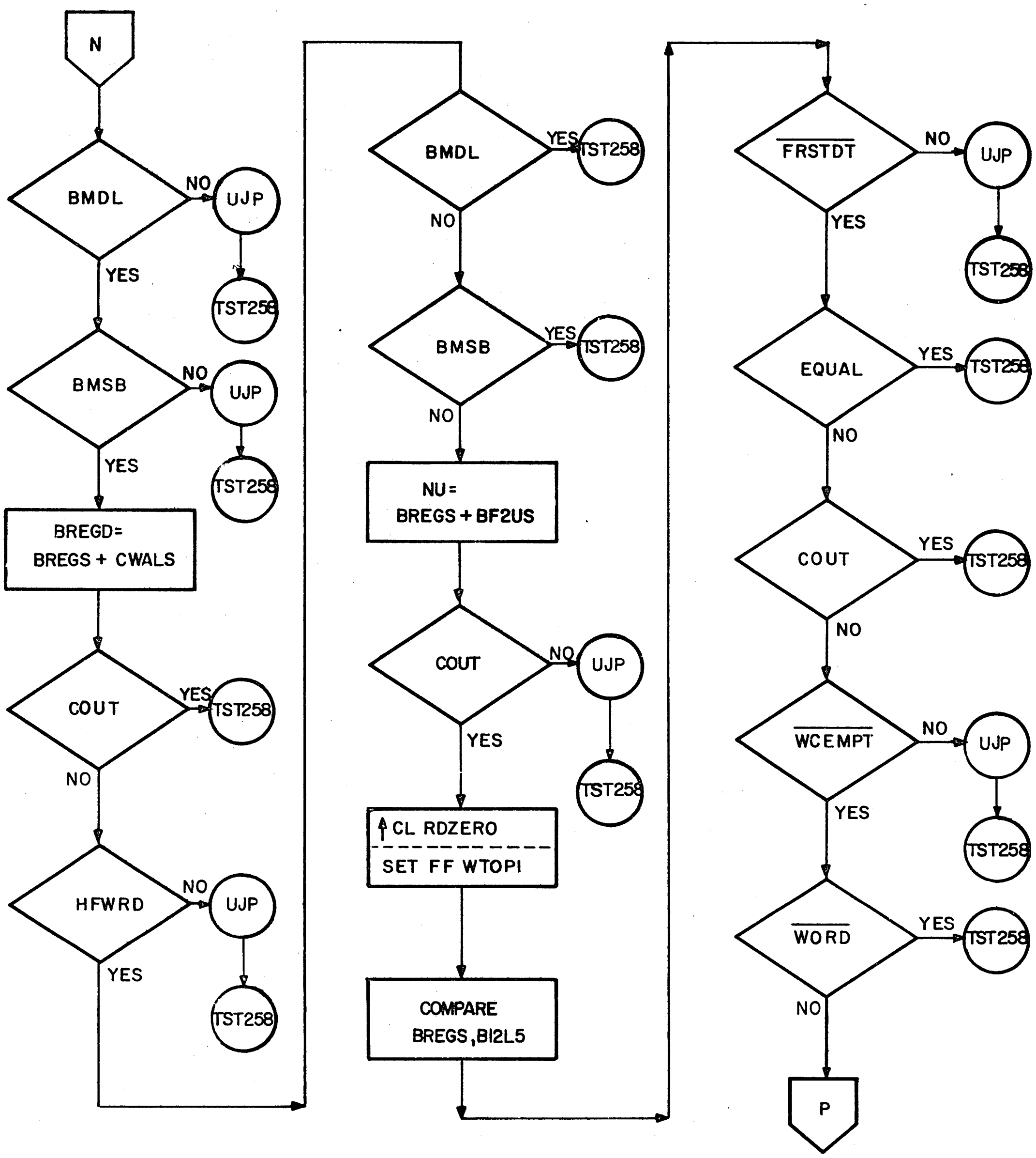
AUTOLOAD and OFFLINE PREPARATIONS ROUTINE



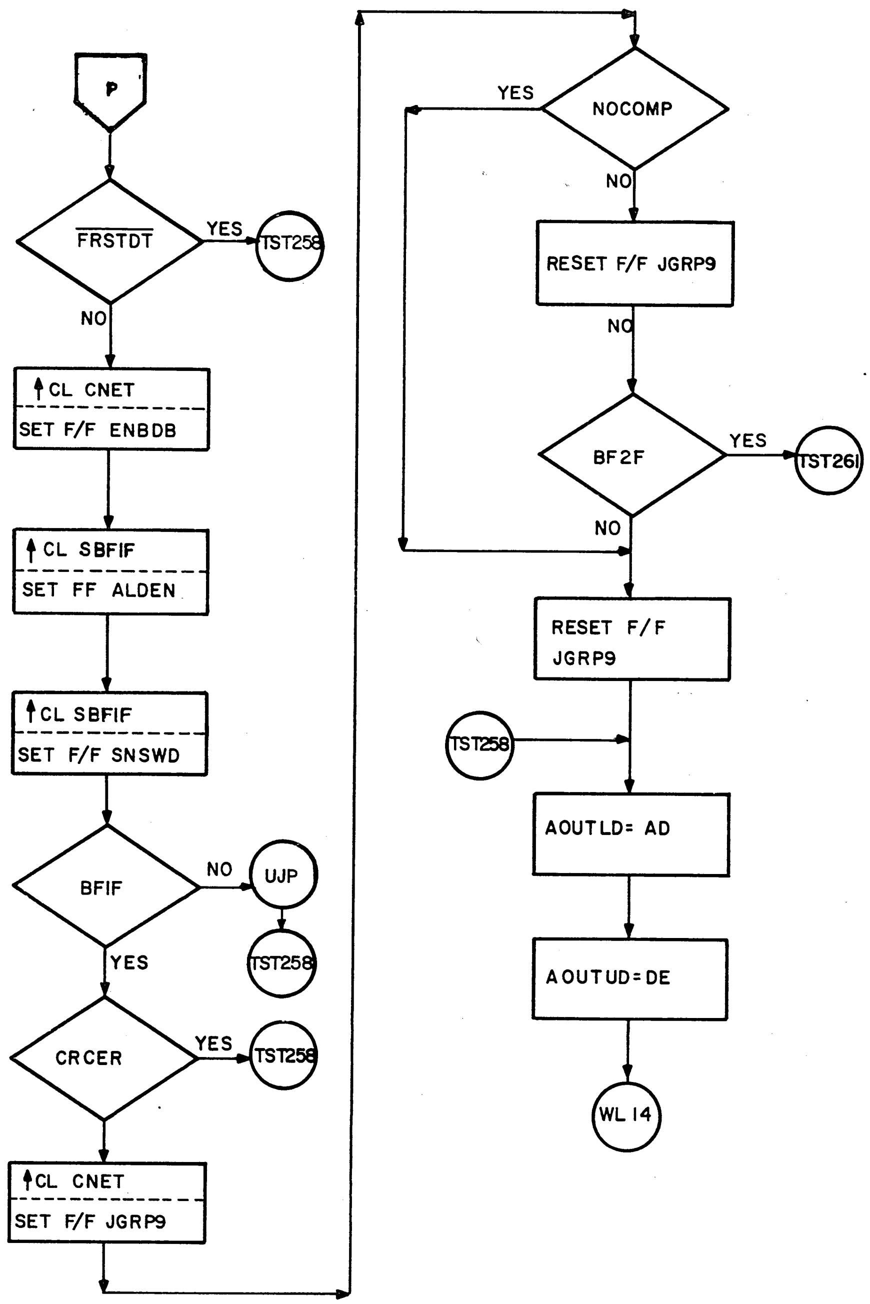
AUTOLOAD AND OFFLINE PREPARATIONS ROUTINE (Continued)



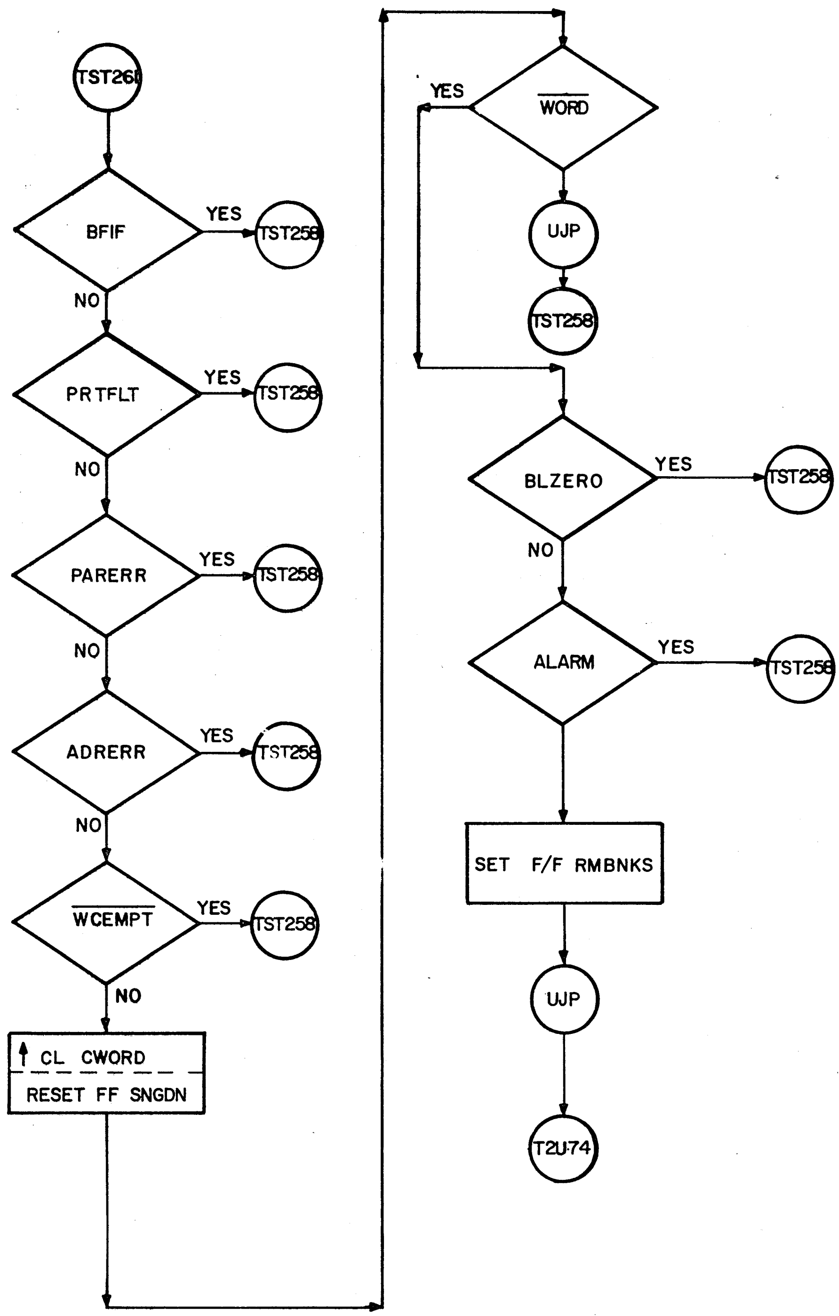
SELF TEST 2 LOWER SECTION



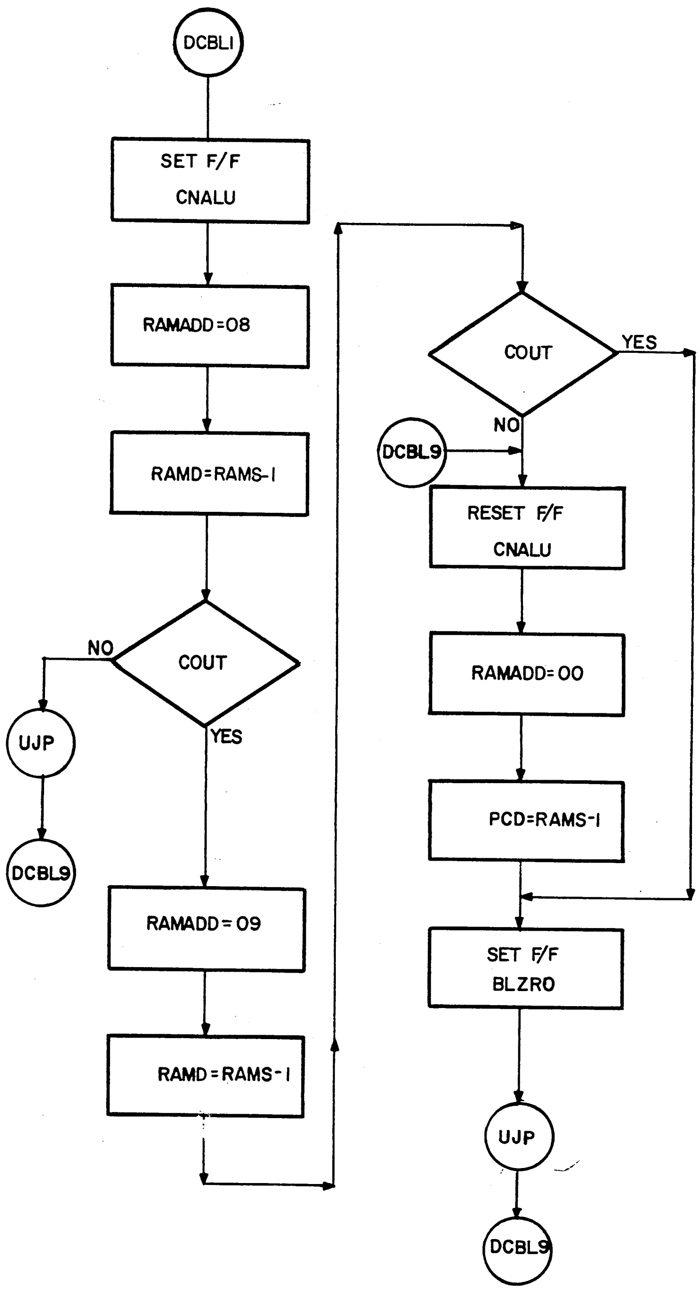
SELF TEST 2 LOWER SECTION (Continued)



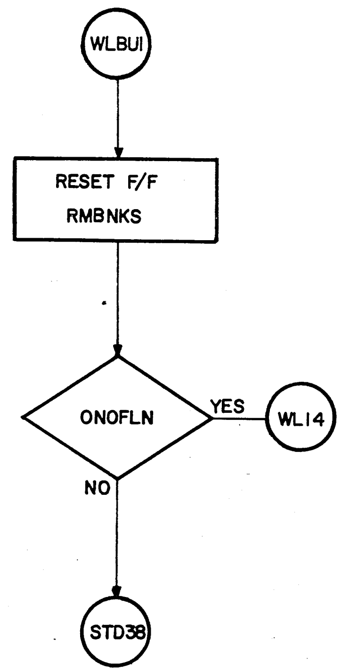
SELF TEST 2 LOWER SECTION (Continued)



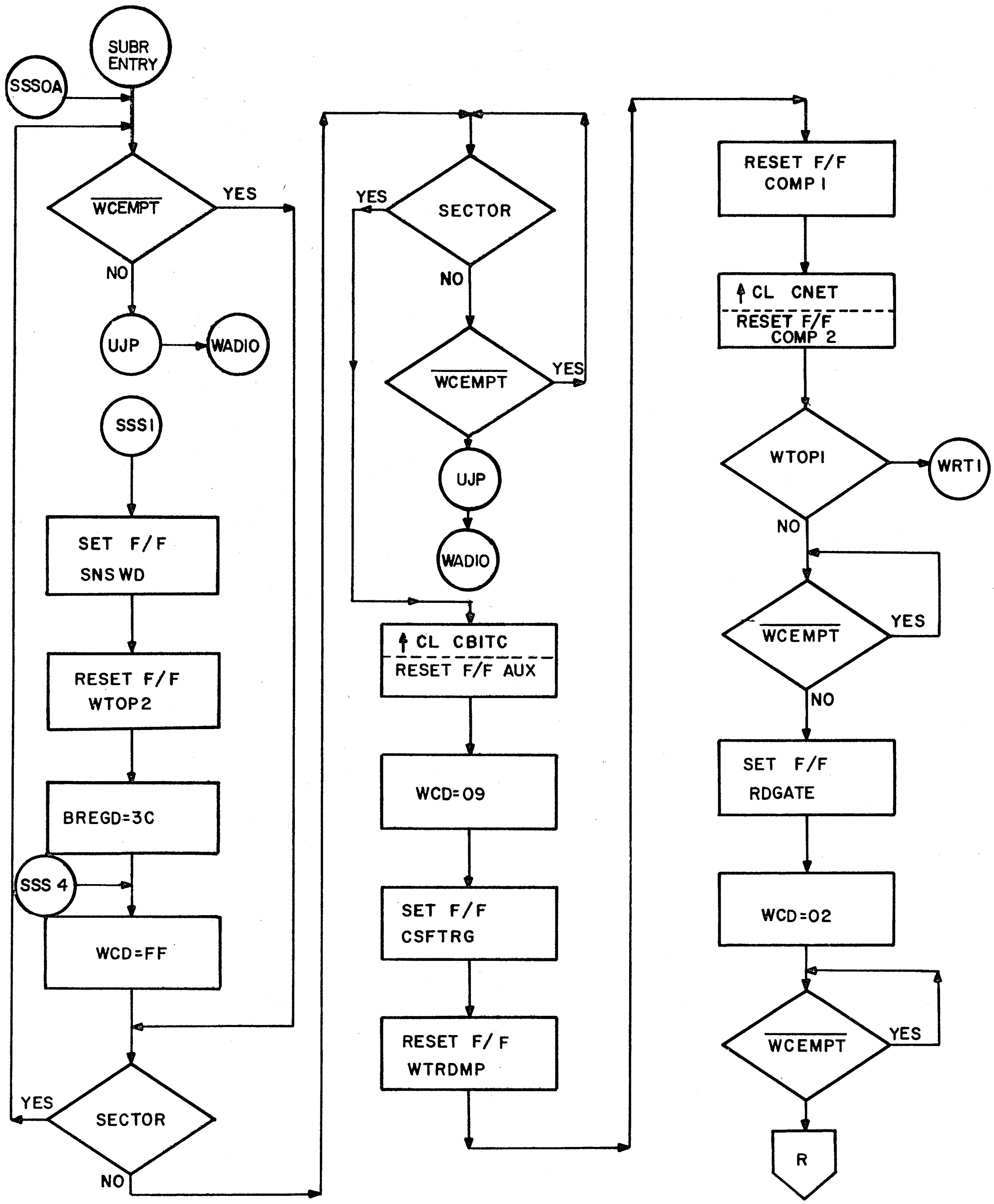
SELF TEST 2 LOWER SECTION (Continued)



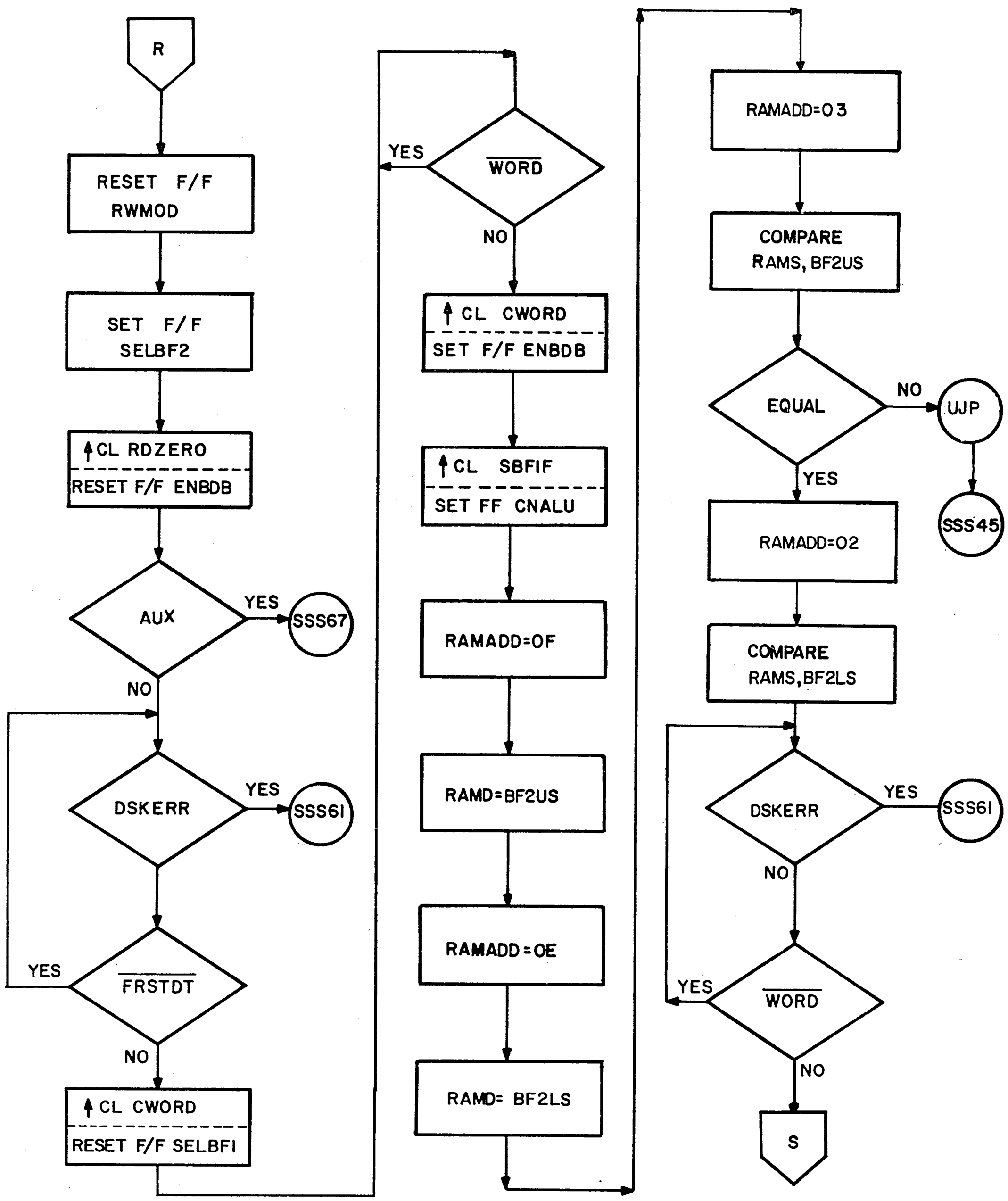
DECREMENT BLOCK LENGTH
SUBROUTINE



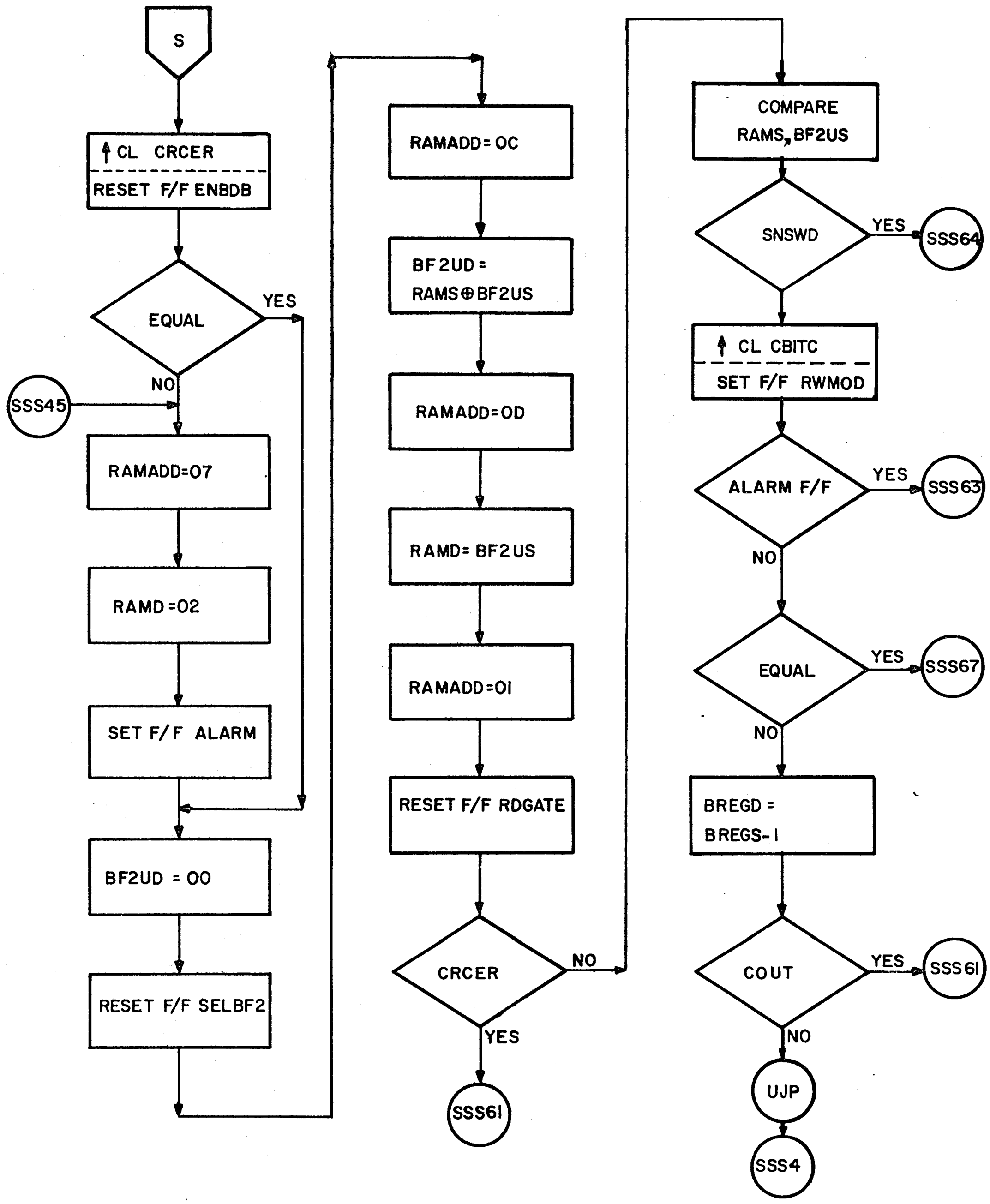
WAITING LOOP
UPPER SECTION



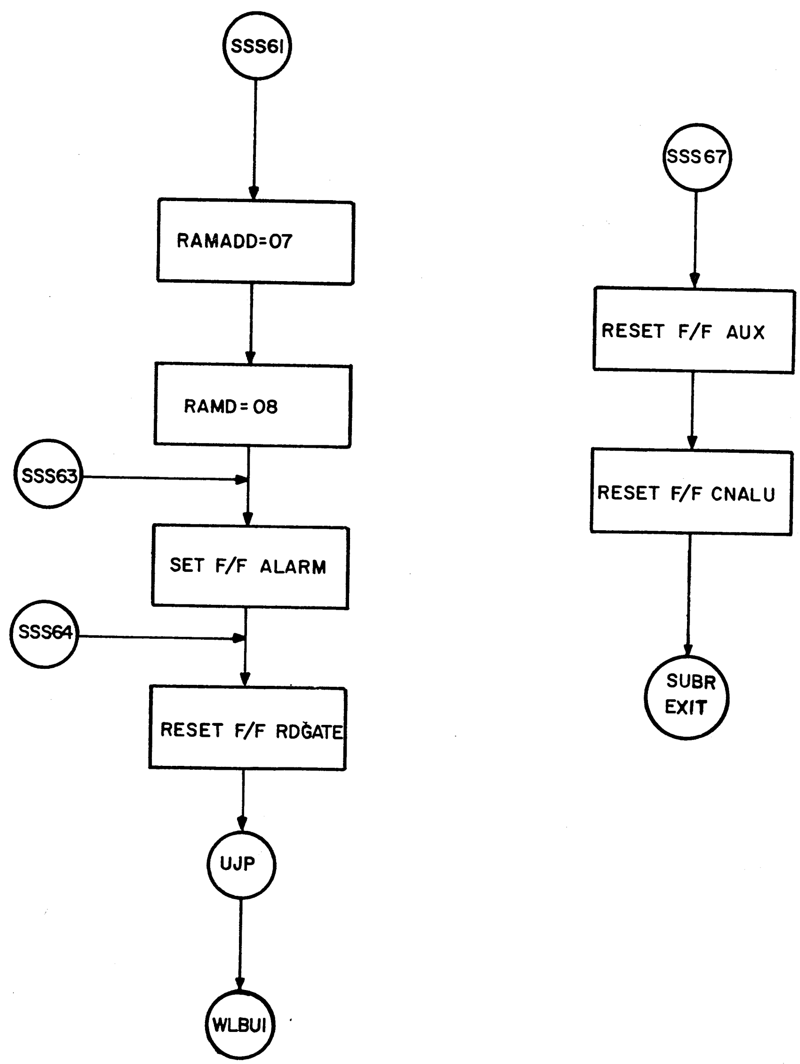
SEARCH SECTOR SUBROUTINE



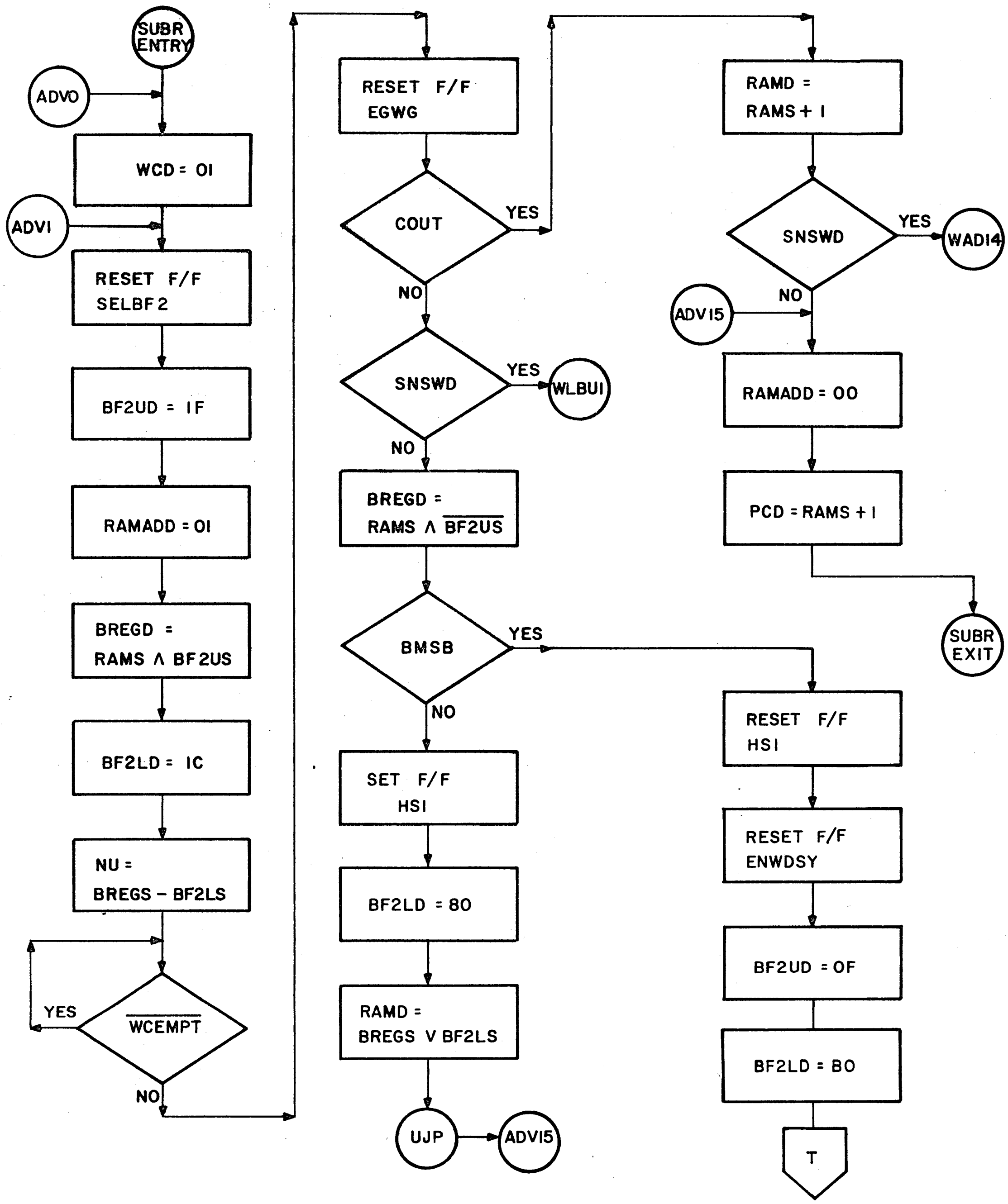
SEARCH SECTOR SUBROUTINE (Continued)



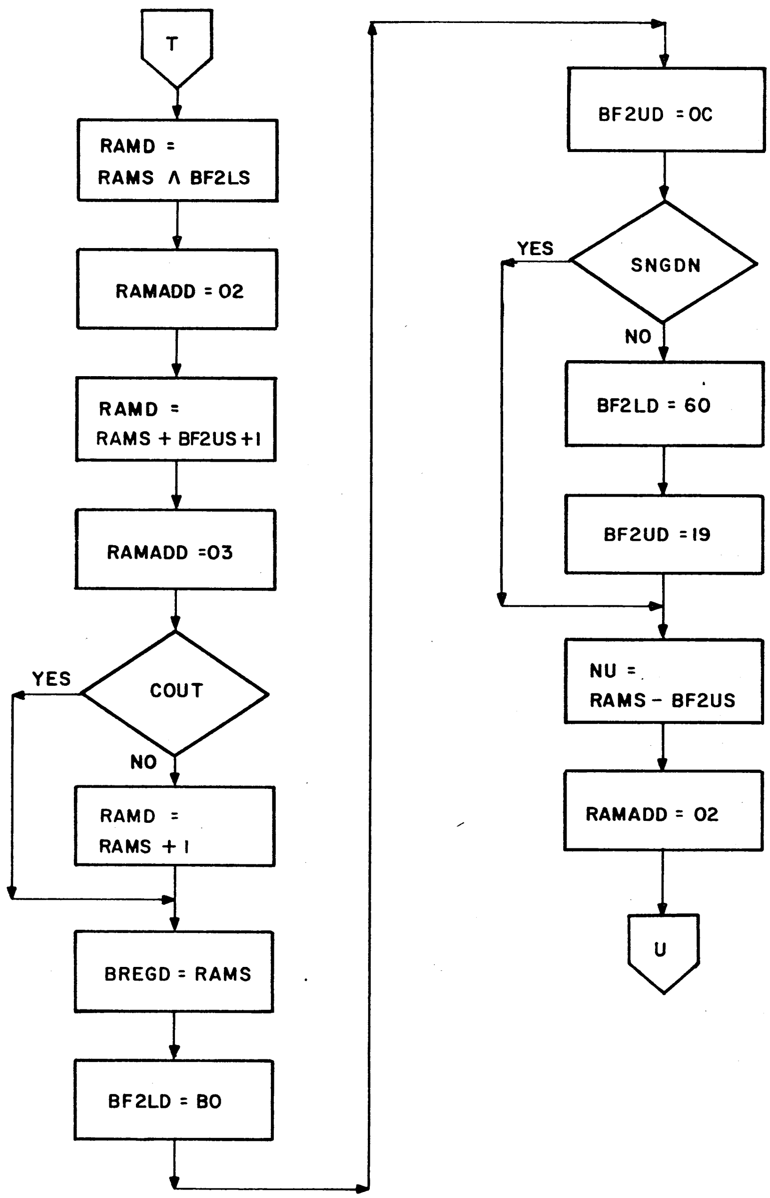
SEARCH SECTOR SUBROUTINE (Continued)



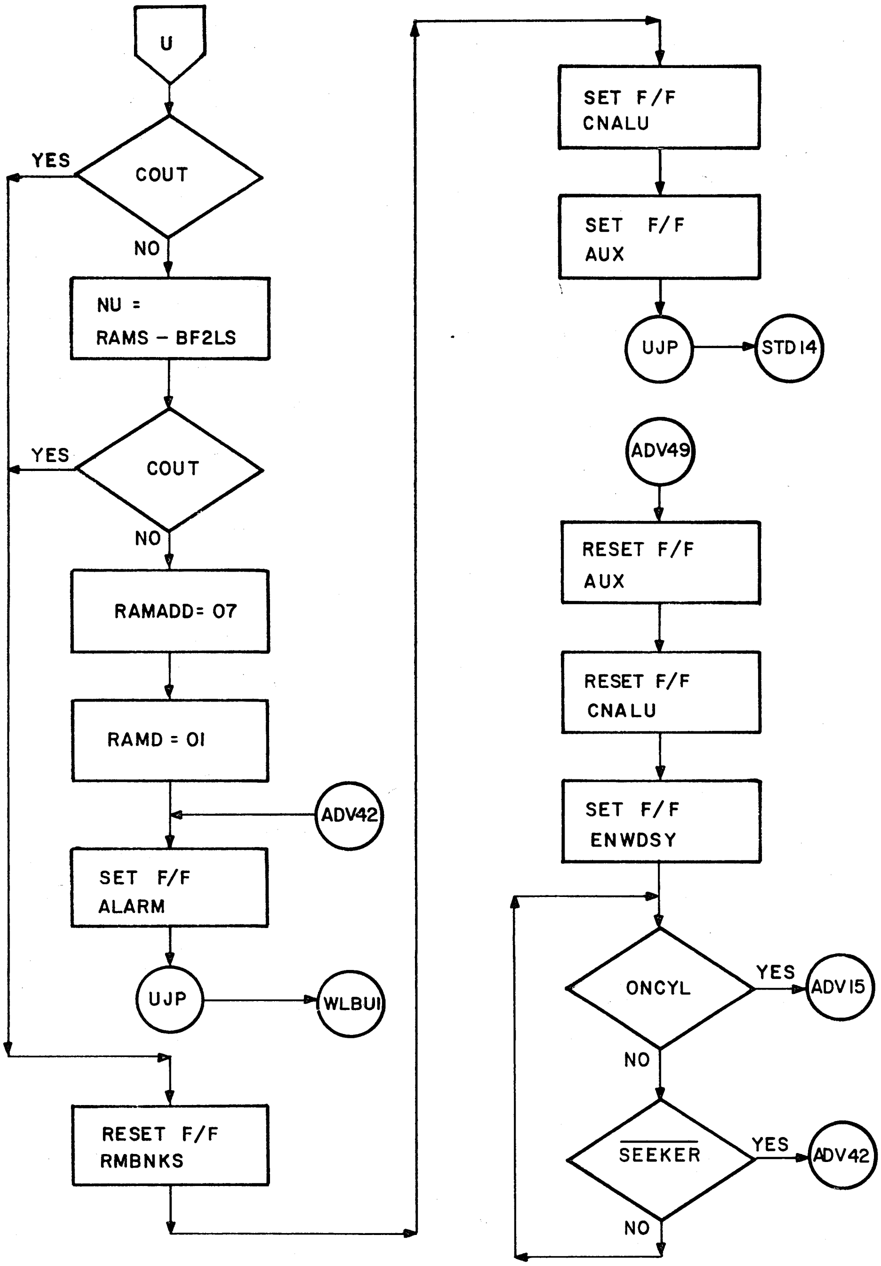
SEARCH SECTOR SUBROUTINE (Continued)



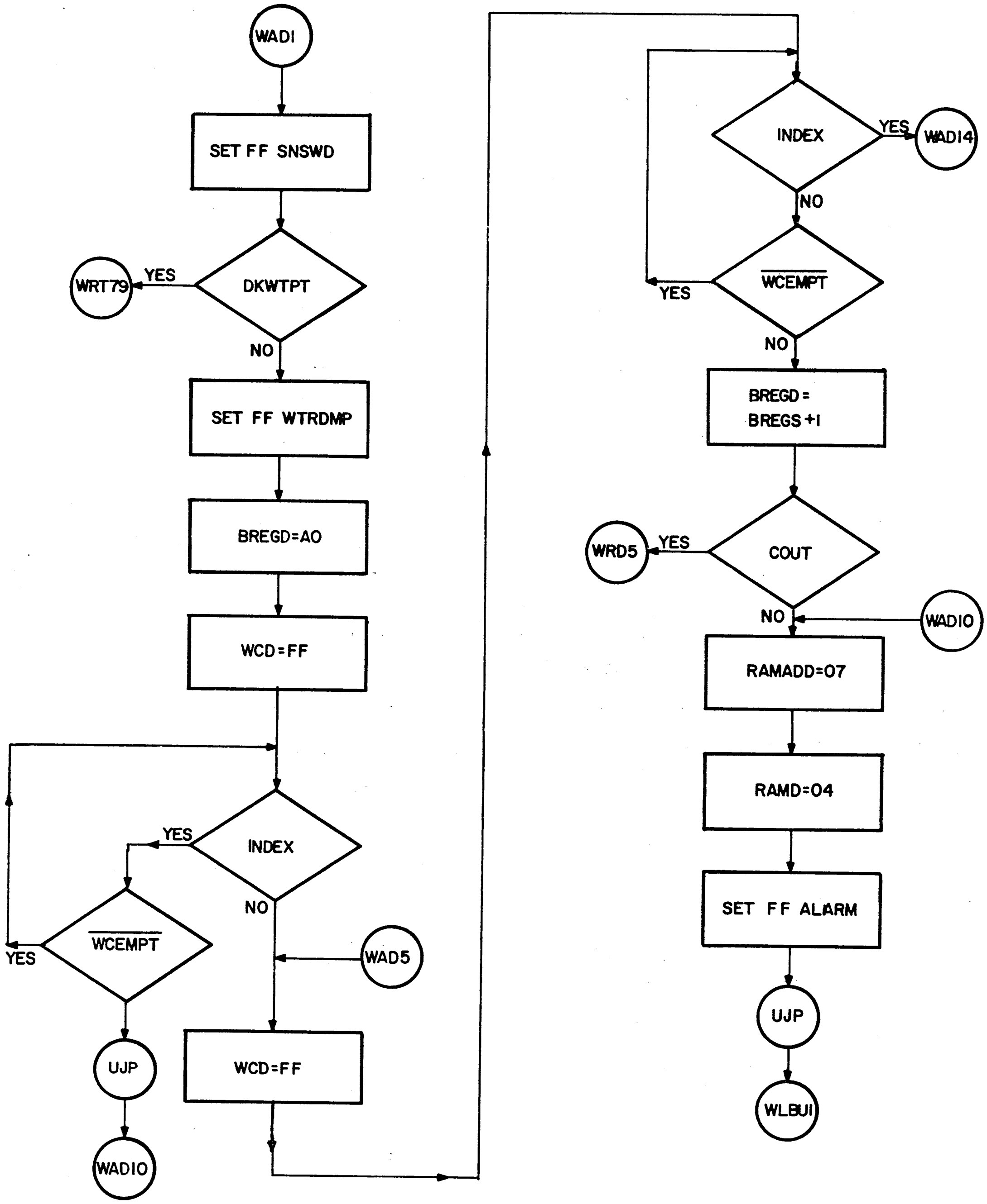
ADVANCE SUBROUTINE



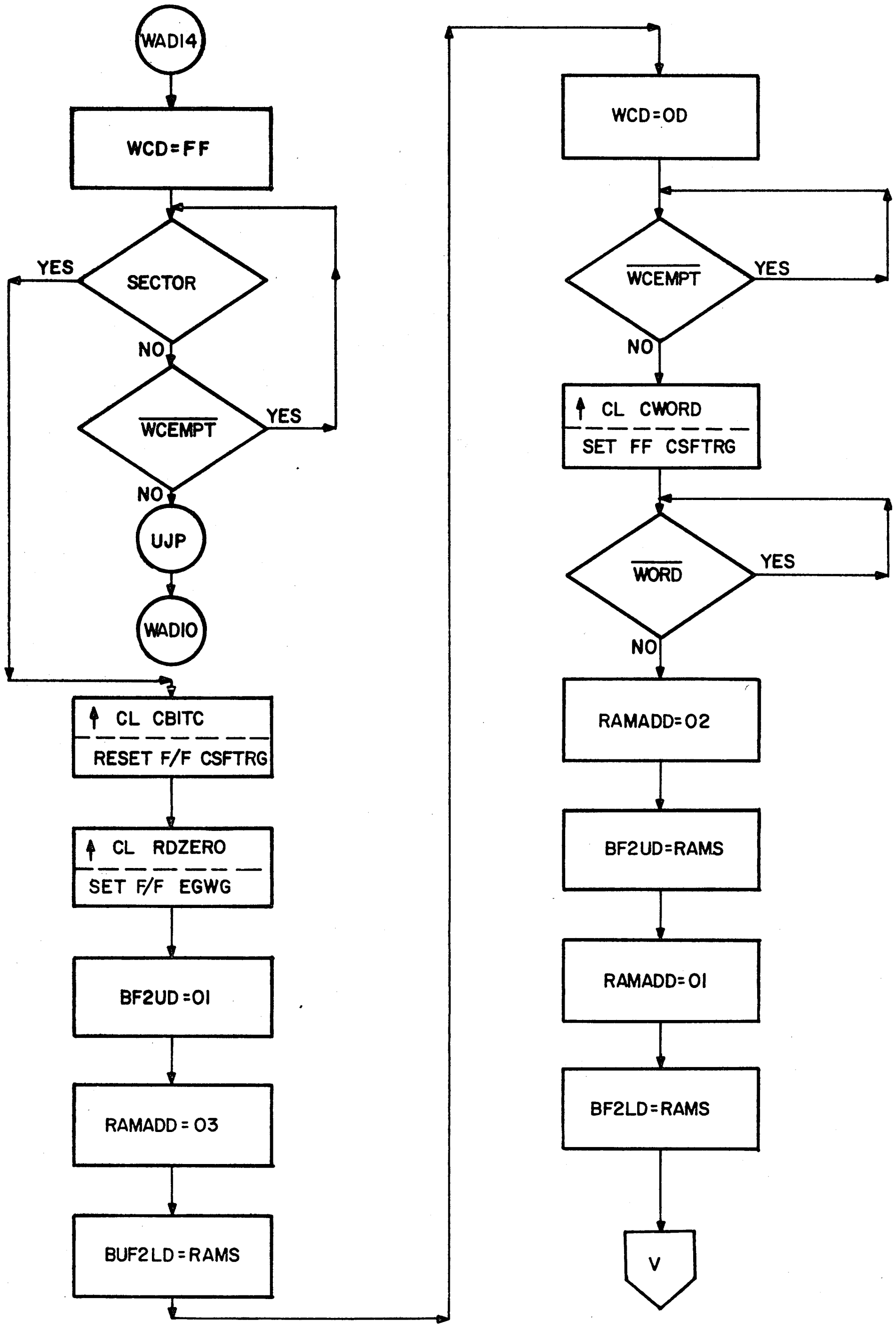
ADVANCE SUBROUTINE (Continued)



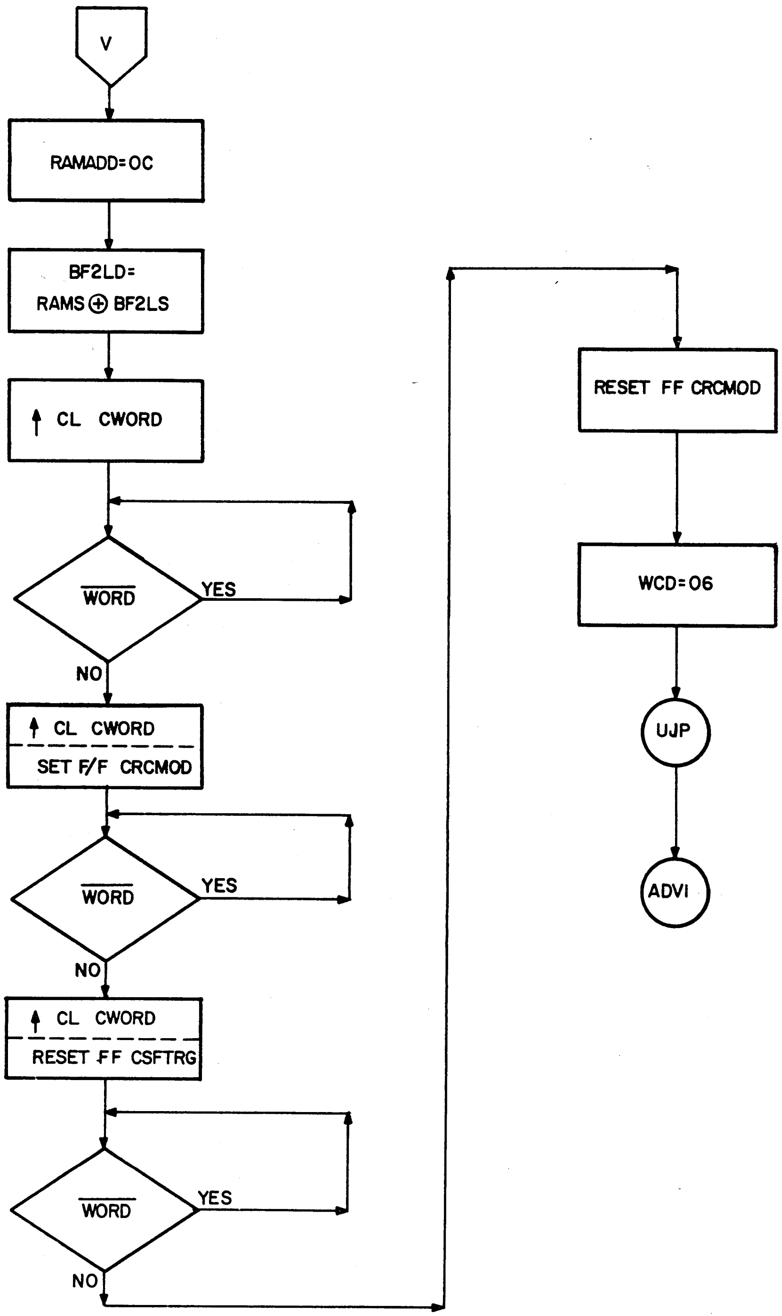
ADVANCE SUBROUTINE (Continued)



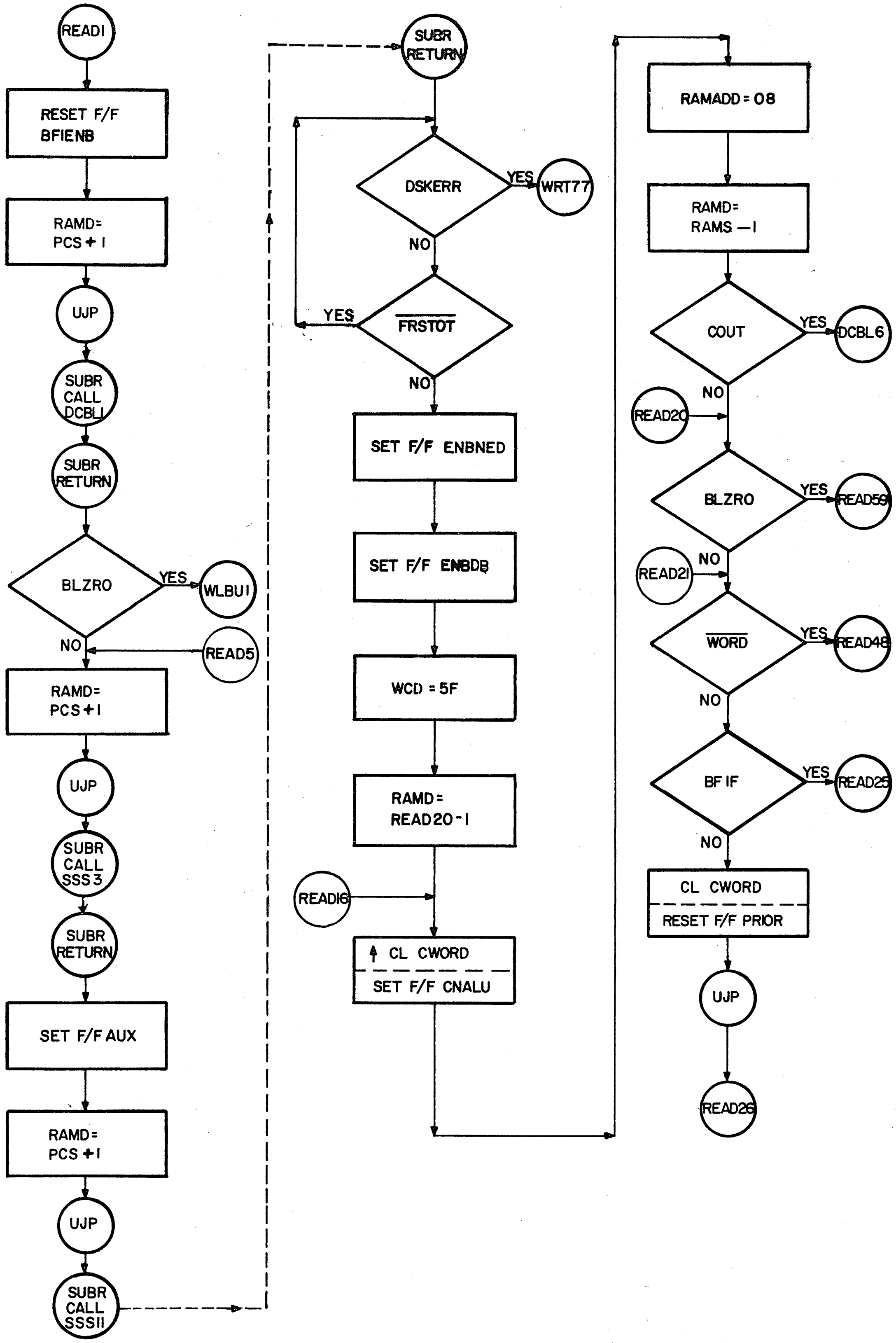
WRITE ADDRESS COMMAND



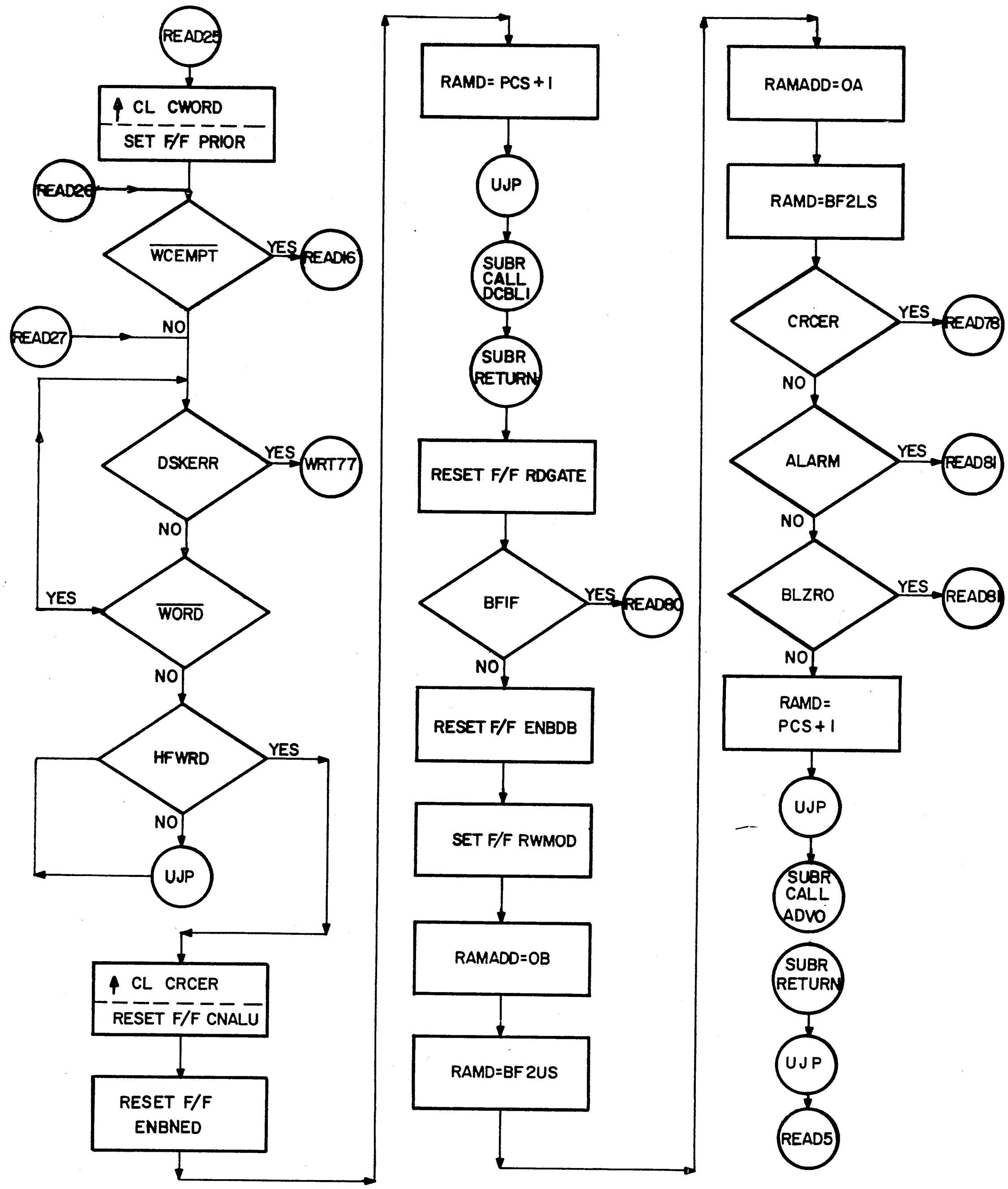
WRITE ADDRESS COMMAND (Continued)



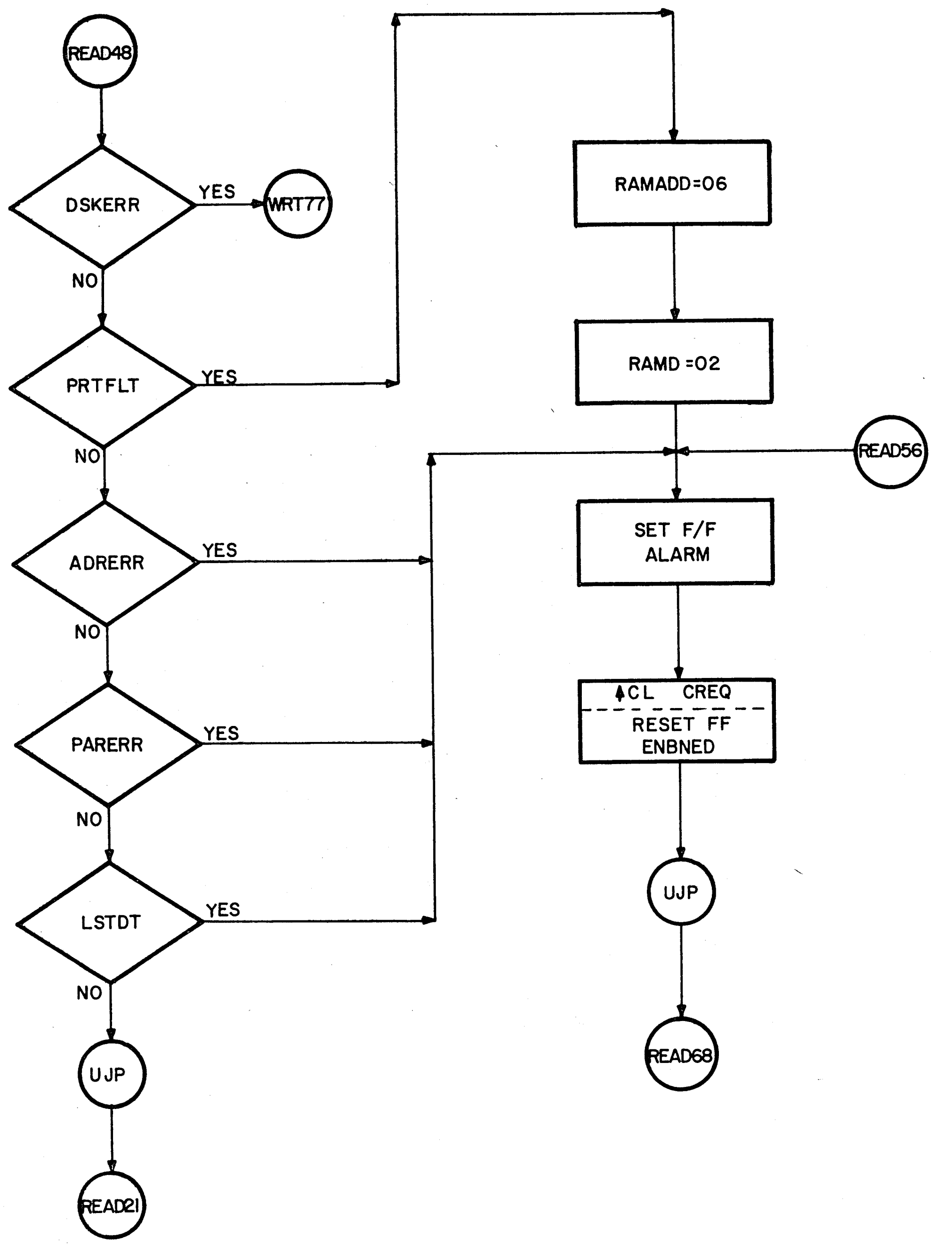
WRITE ADDRESS COMMAND (Continued)



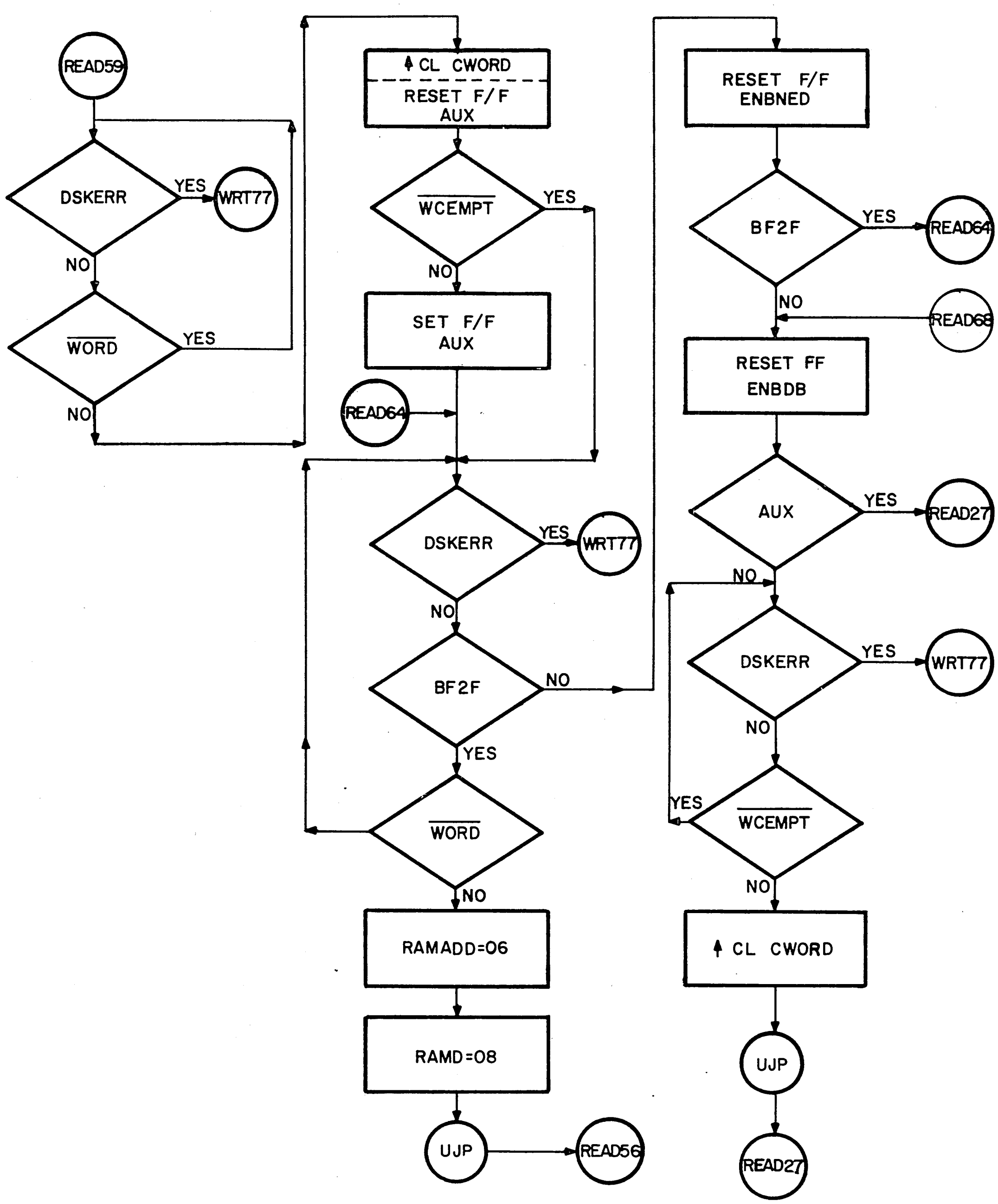
READ AND CHECKWORD CHECK COMMANDS



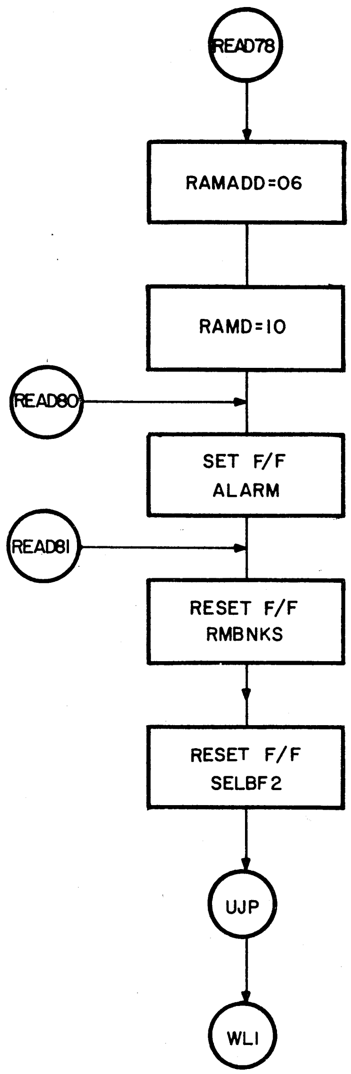
READ AND CHECKWORD CHECK COMMANDS (Continued)



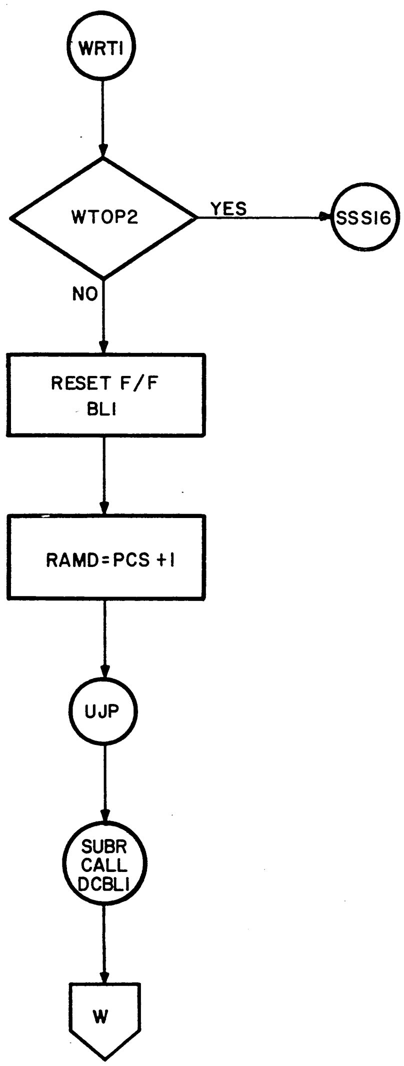
READ AND CHECKWORD CHECK COMMANDS (Continued)



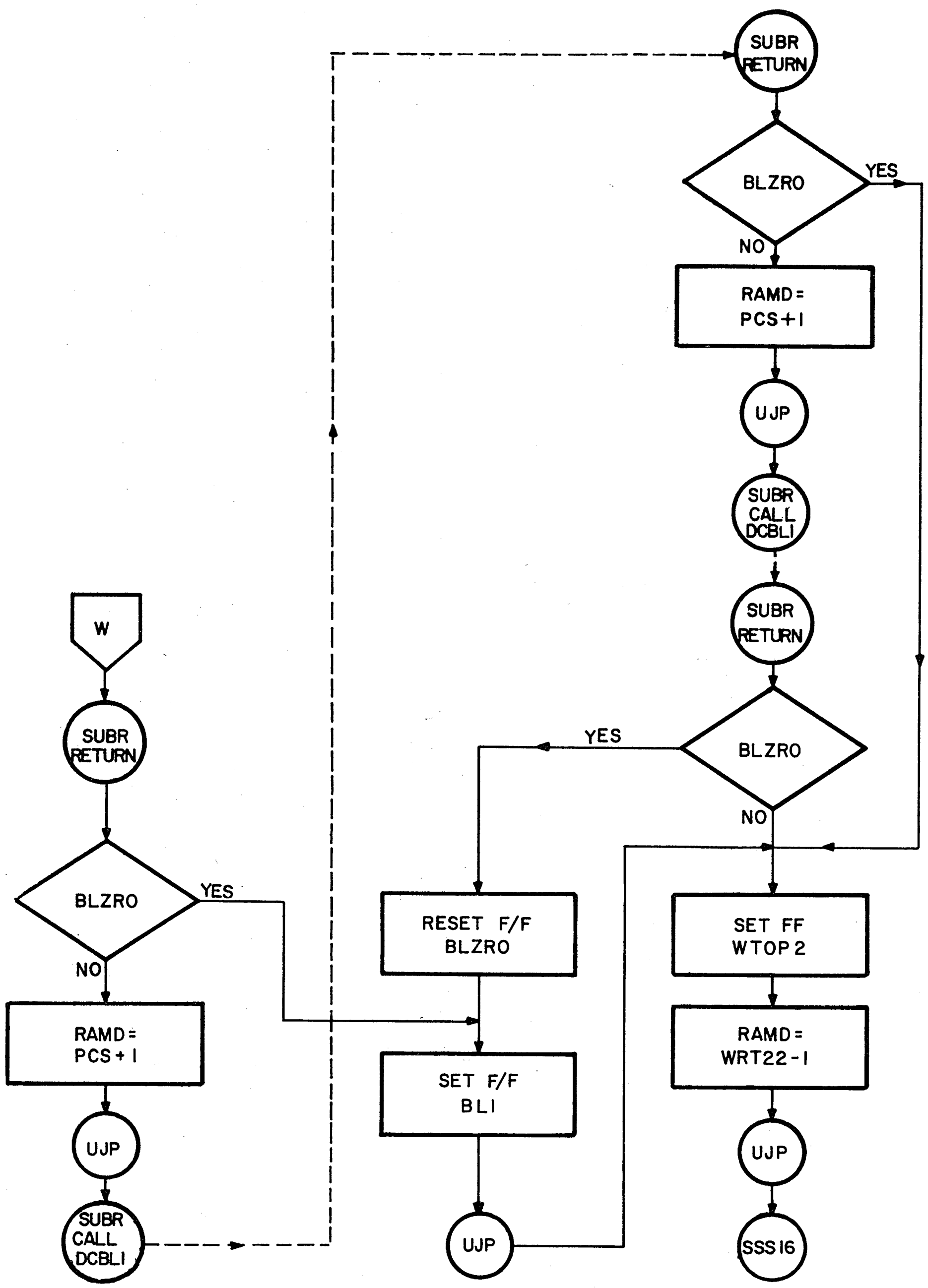
READ AND CHECKWORD CHECK COMMANDS (Continued)



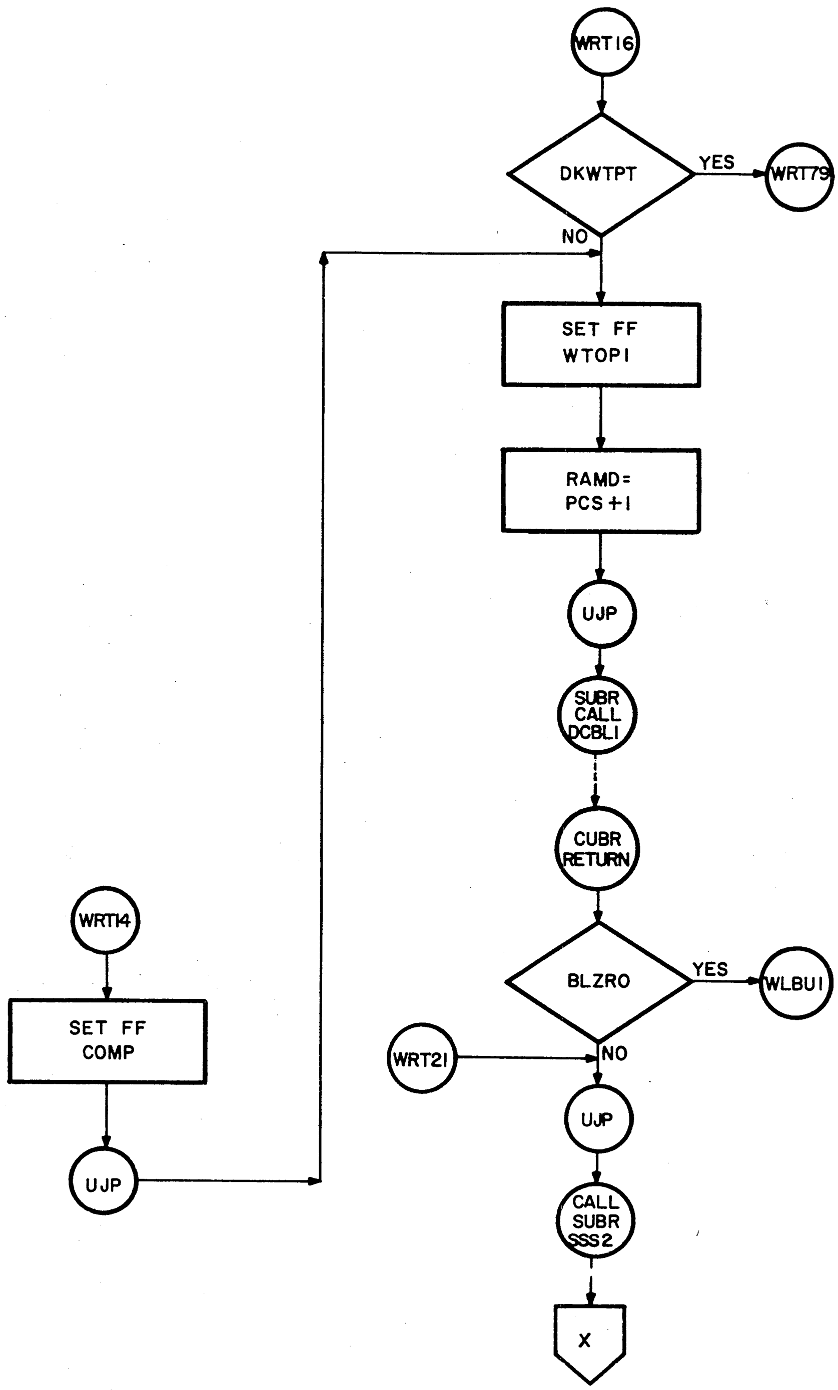
READ AND CHECKWORD CHECK COMMANDS (Continued)



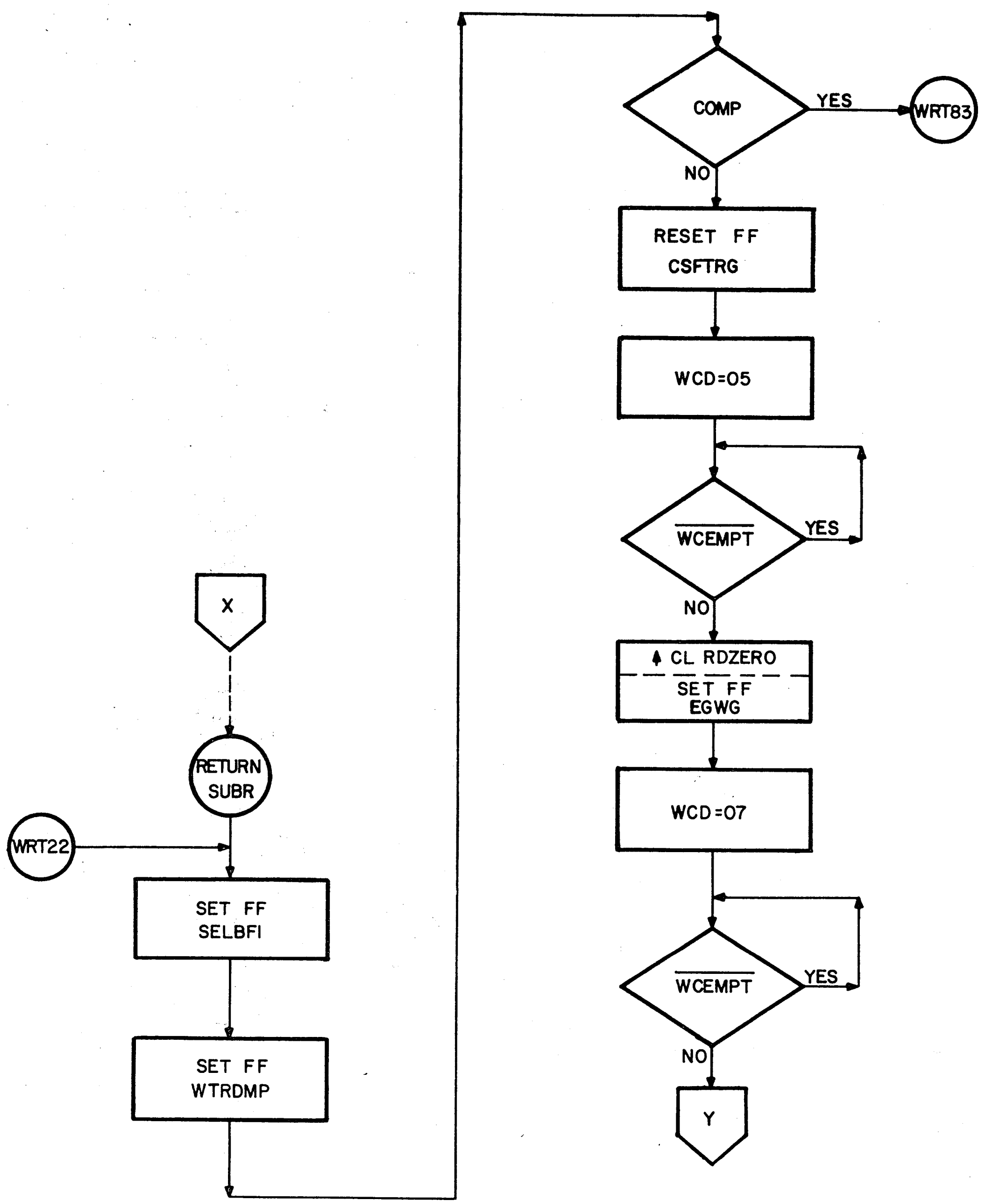
WRITE DATA and COMPARE COMMANDS



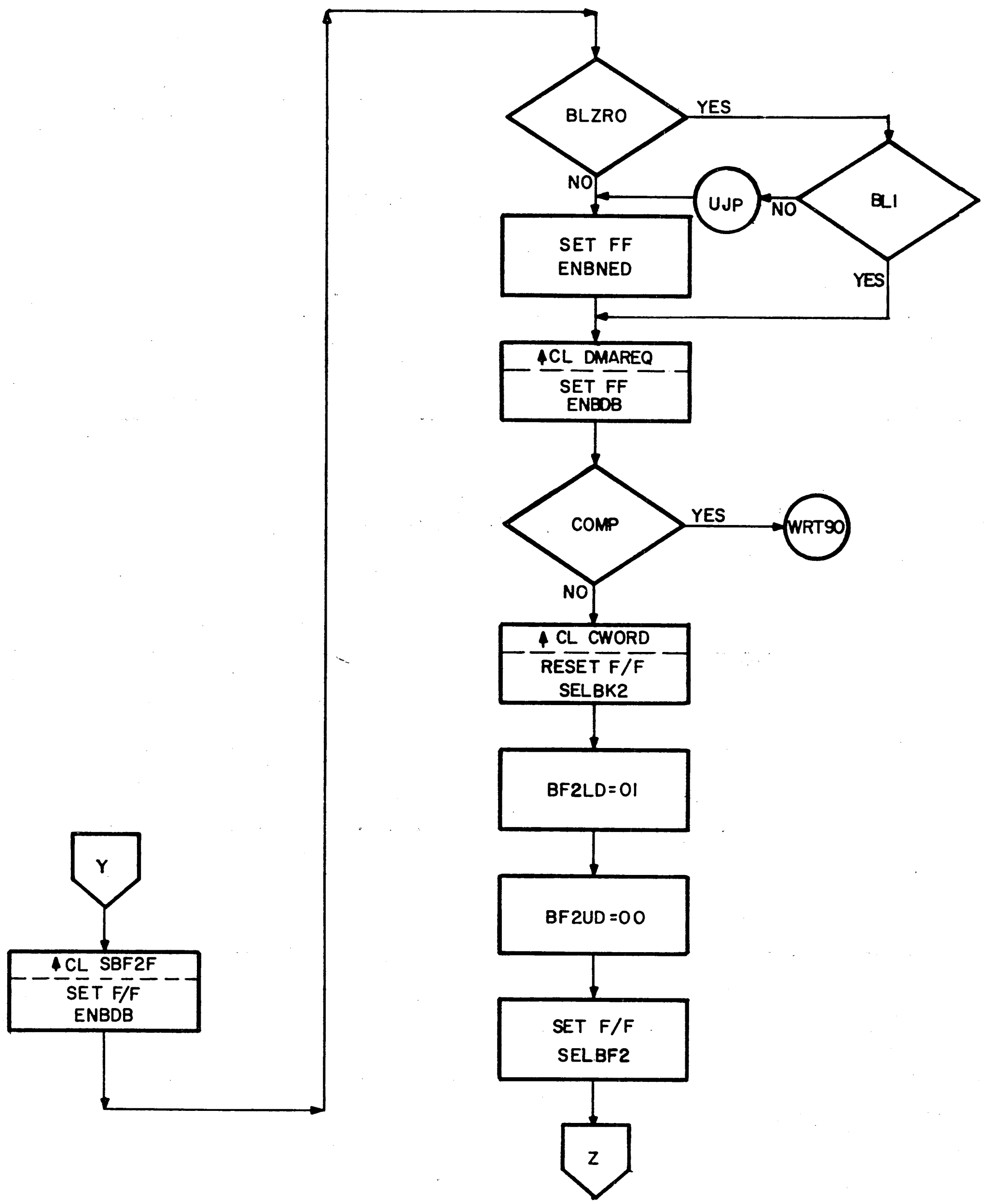
WRITE DATA and COMPARE
COMMANDS (Continued)



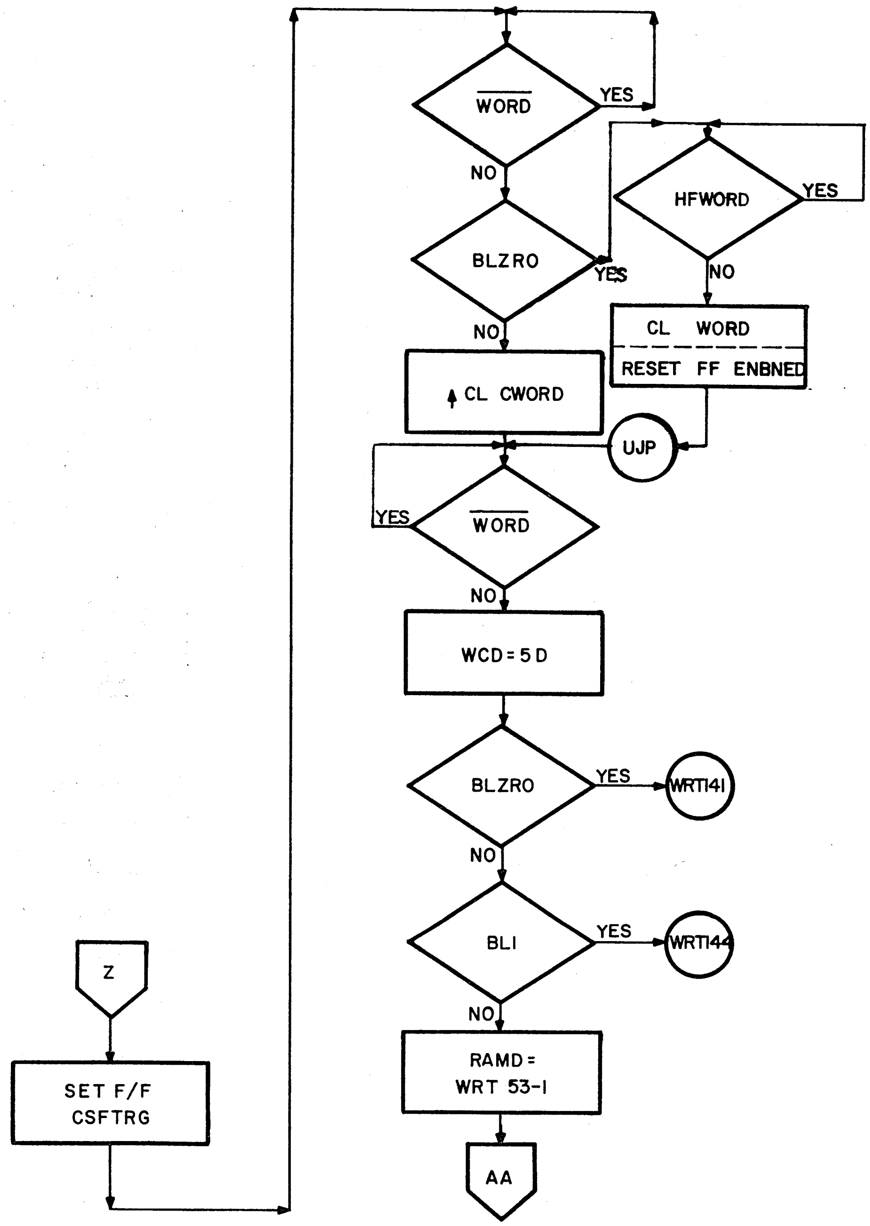
WRITE DATA and COMPARE
COMMANDS (Continued)



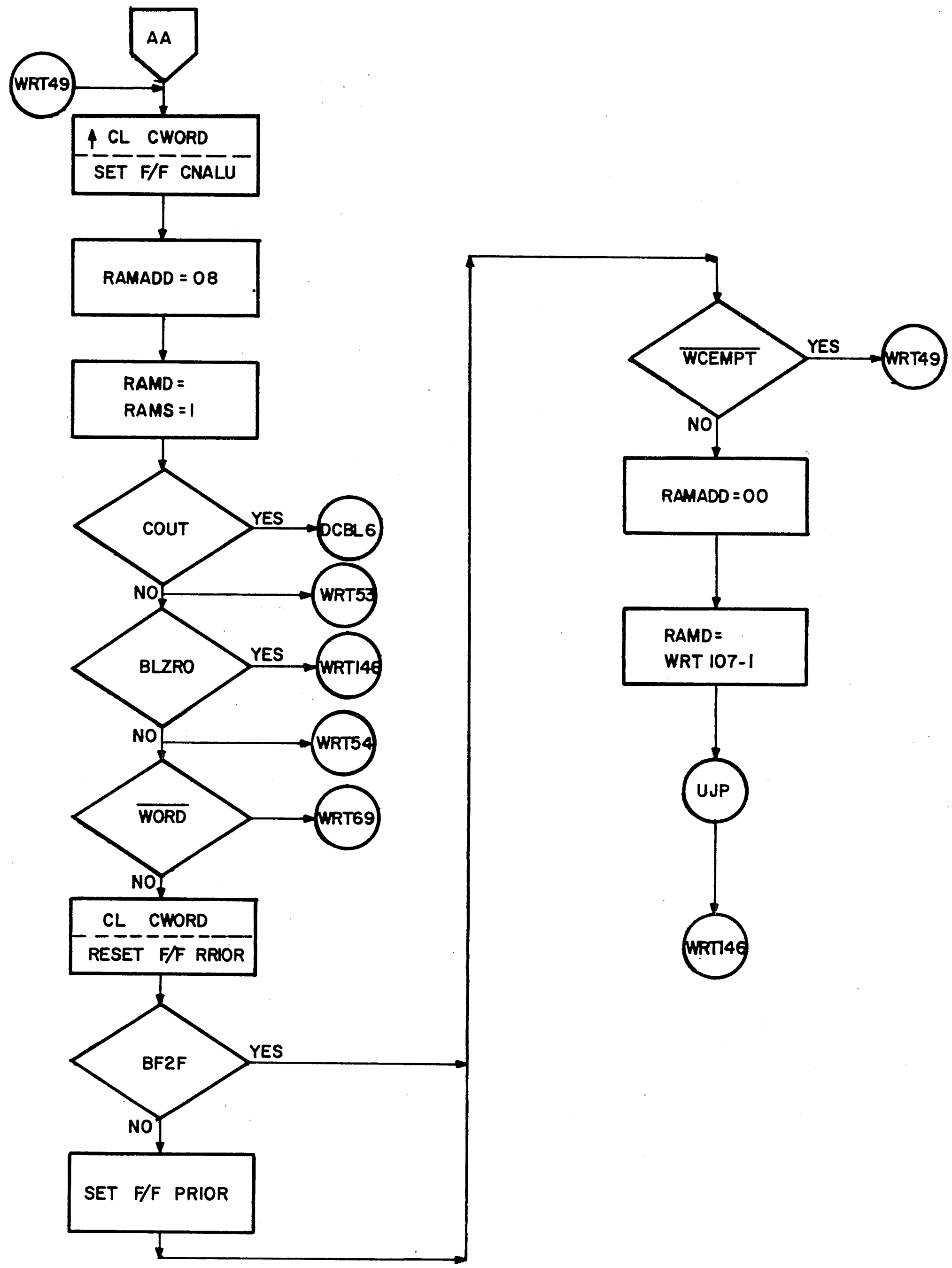
WRITE DATA and COMPARE
COMMANDS (Continued)



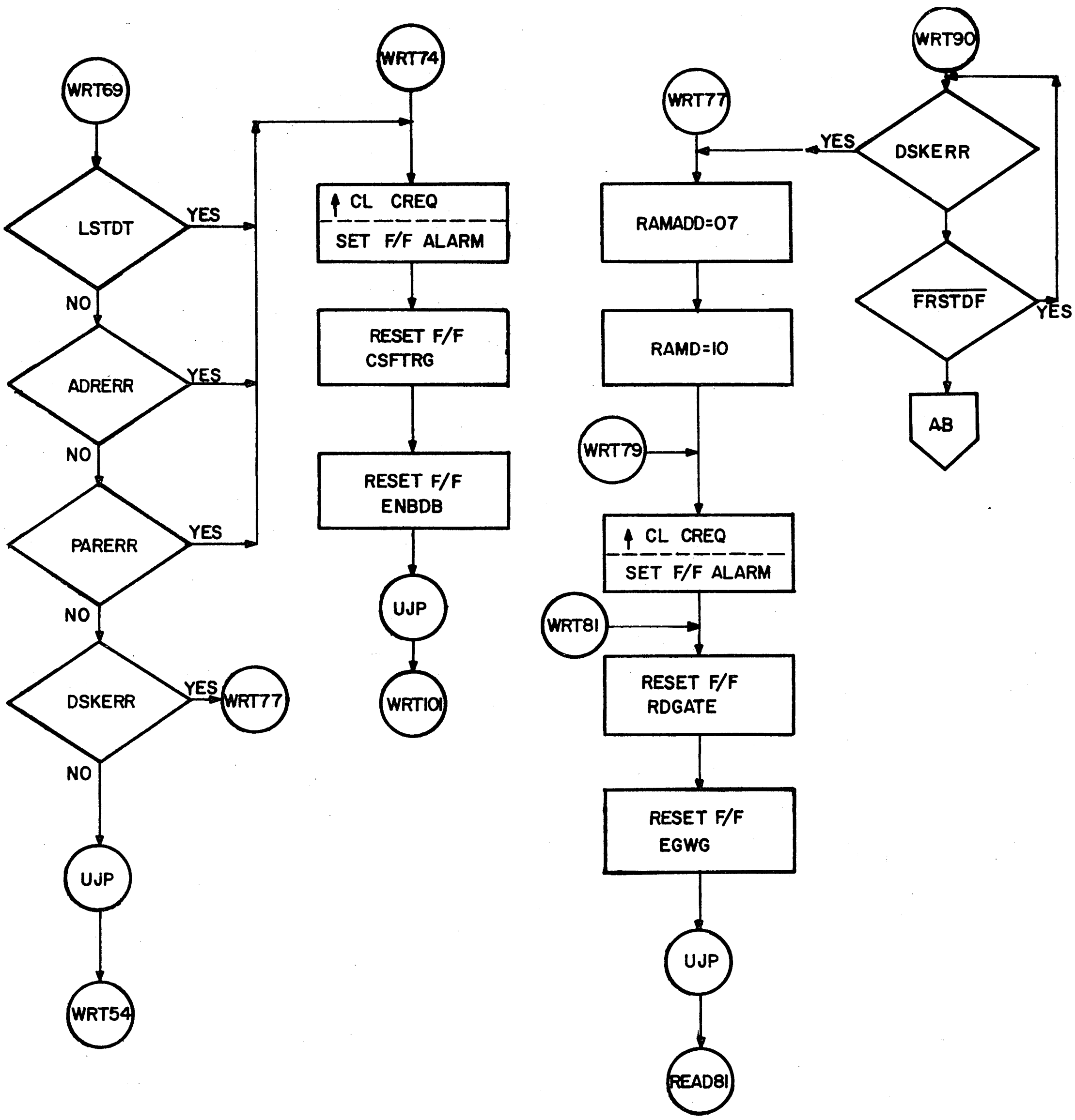
WRITE DATA and COMPARE
COMMANDS (Continued)



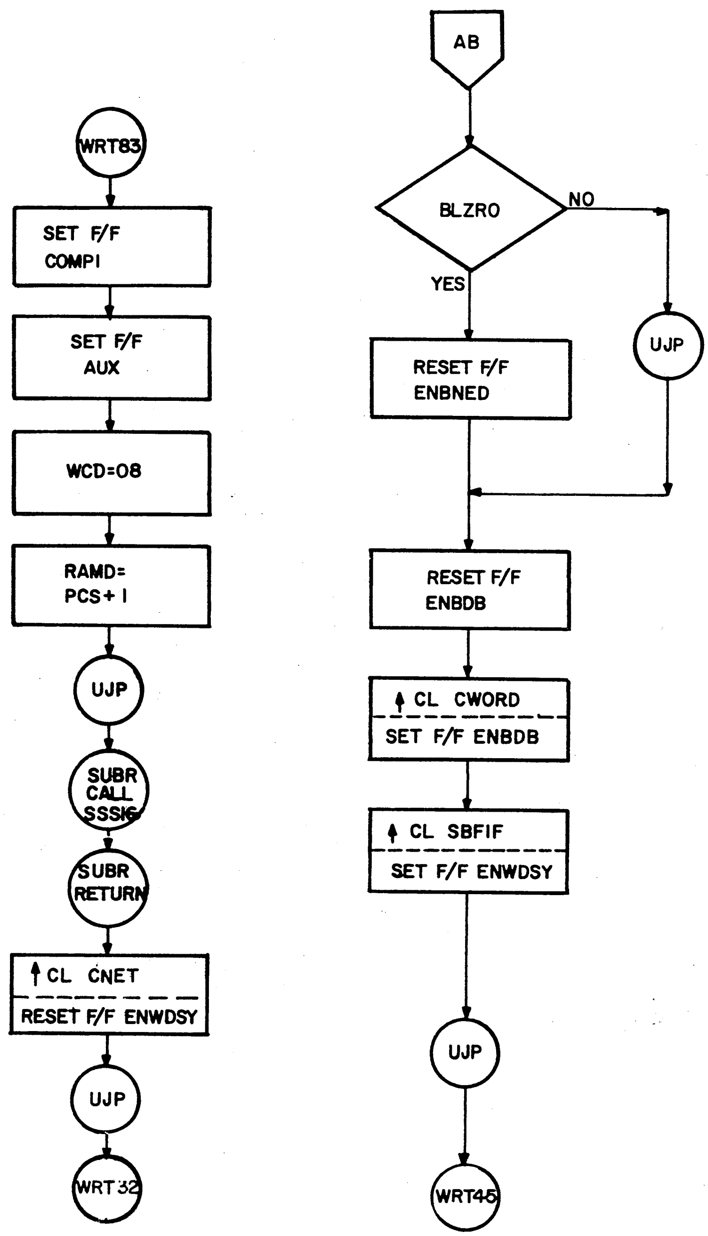
WRITE DATA and COMPARE
COMMANDS (Continued)



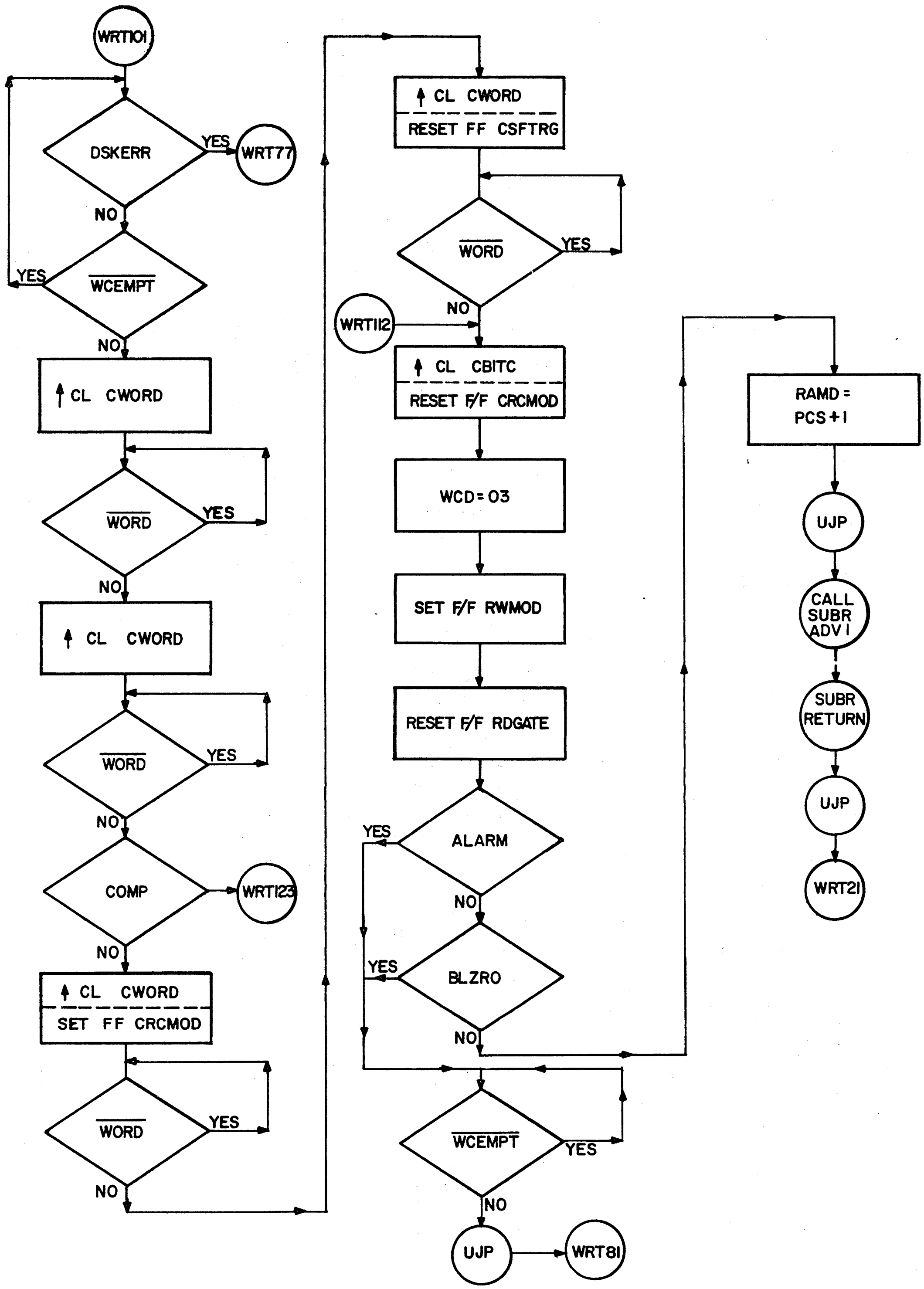
WRITE DATA and COMPARE
COMMANDS (Continued)



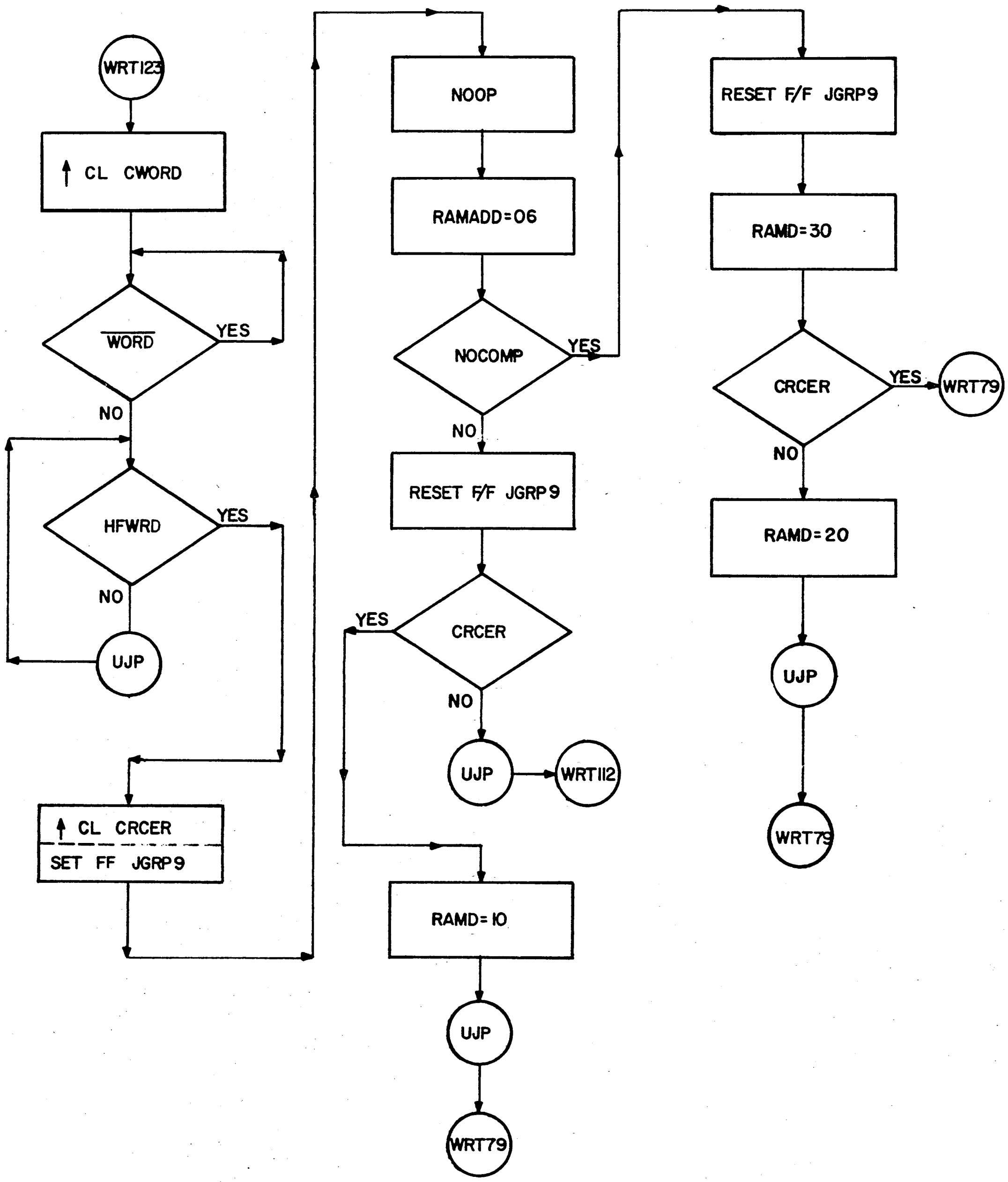
WRITE DATA and COMPARE
COMMANDS (Continued)



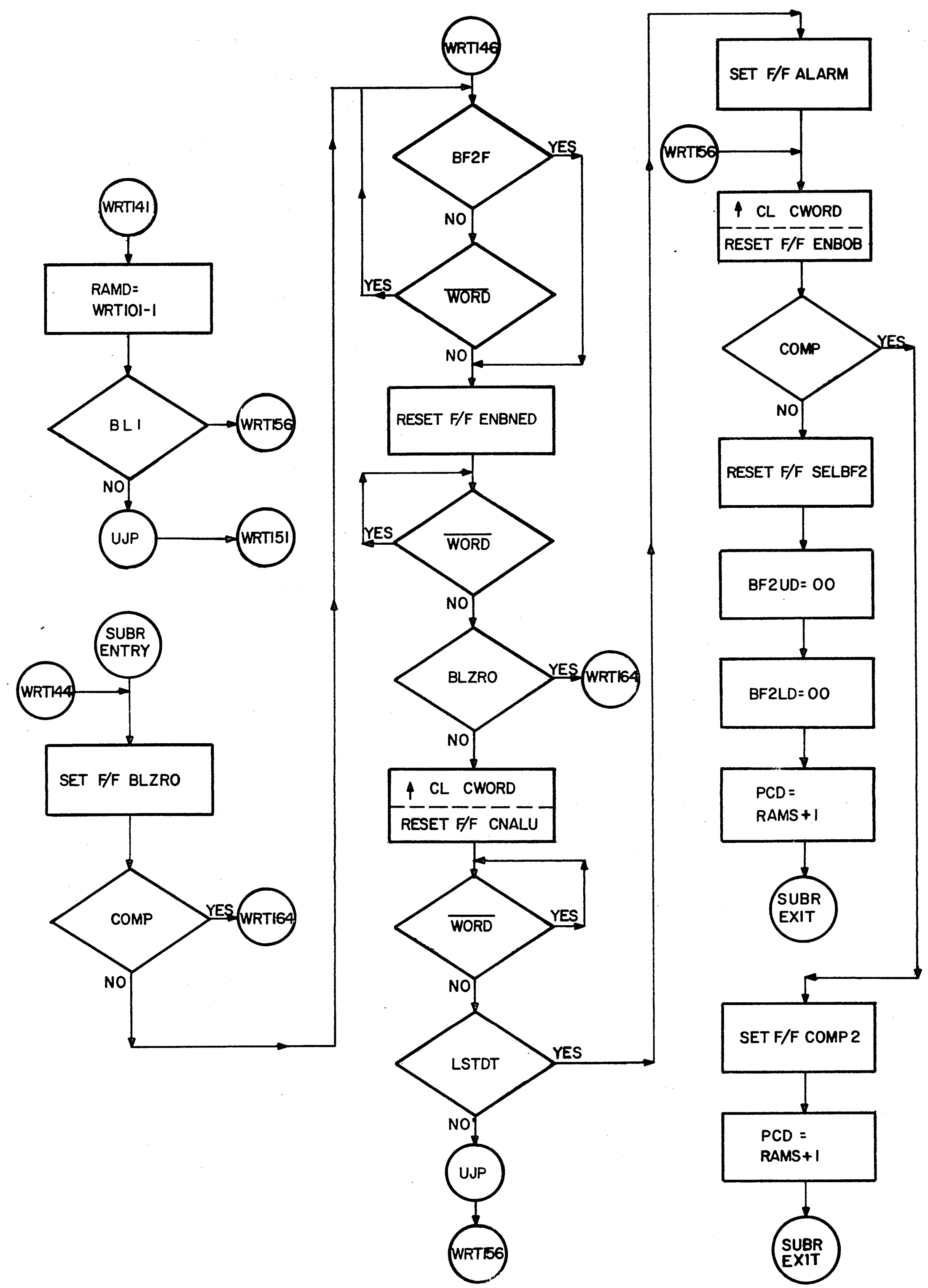
WRITE DATA and COMPARE
COMMANDS (Continued)



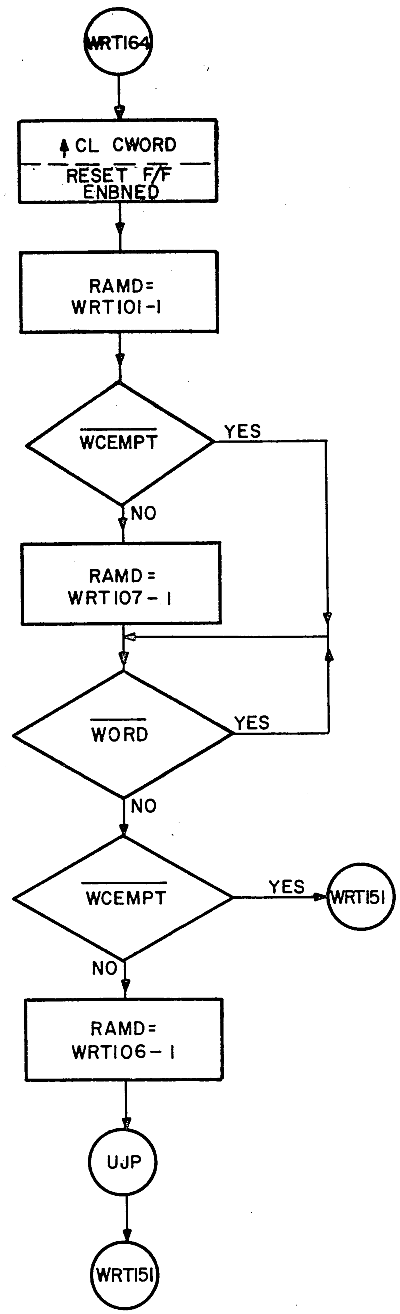
WRITE DATA and COMPARE
COMMANDS (Continued)



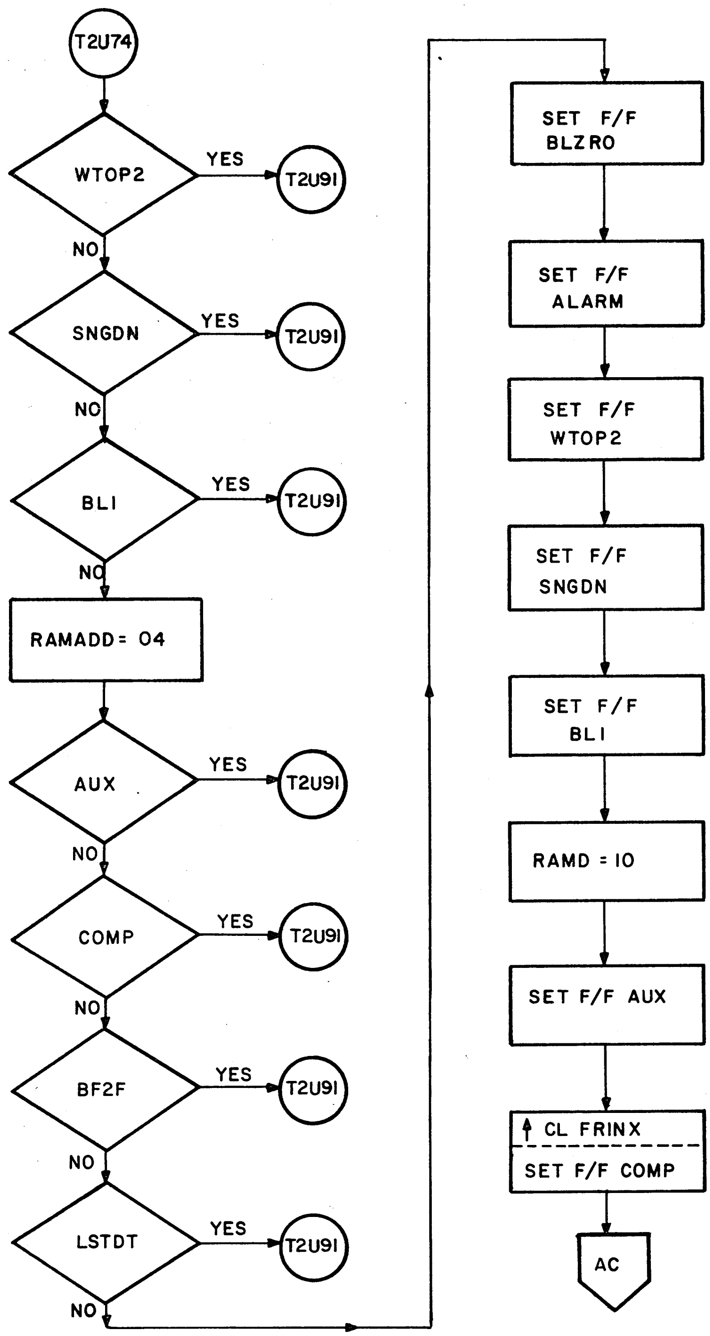
WRITE DATA and COMPARE COMMANDS (Continued)



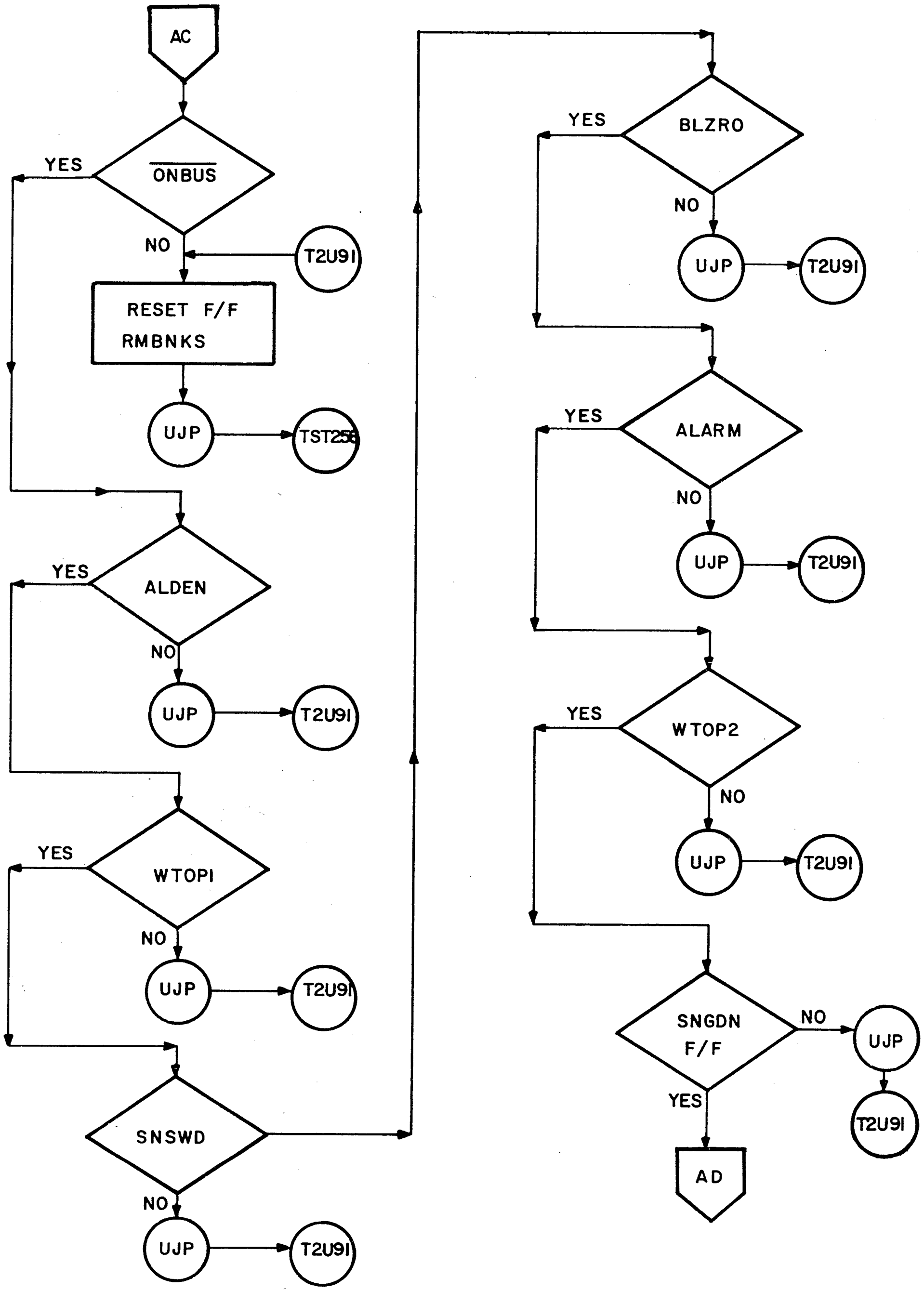
WRITE DATA and COMPARE
COMMANDS (Continued)



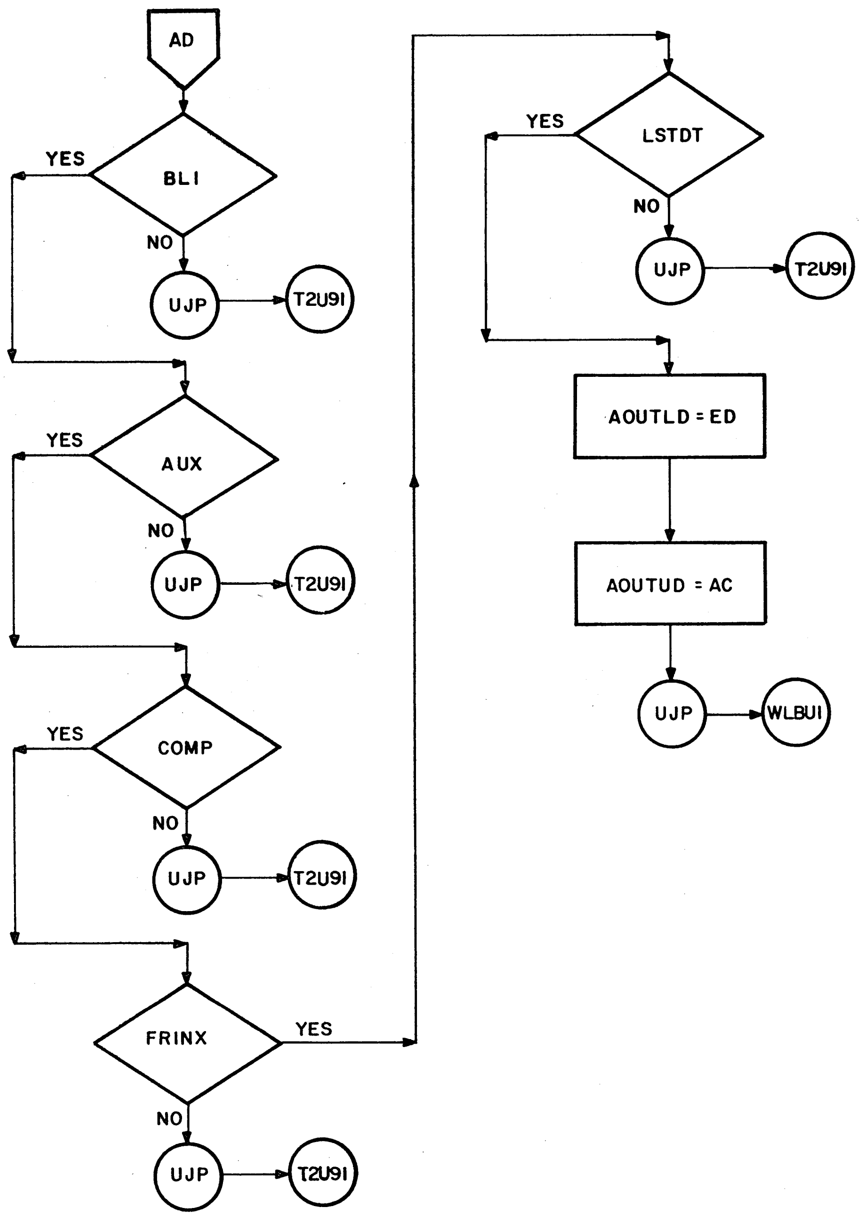
WRITE DATA and COMPARE
COMMANDS (Continued)



SELF TEST 2 UPPER SECTION



SELF TEST 2 UPPER SECTION (Continued)



SELF TEST 2 UPPER SECTION (Continued)

```
FA111A                    PAGE    1              DATE: 04/06/77

                 NAM FA111A

         *****************************************************************
         *****************************************************************
         **                                                             **
         **                 MICRO-PROGRAM ASSEMBLER                     **
         **          CARTRIDGE DISK DRIVE CONTROLLER FA111-A            **
         **                 89601265 REVISION 04                        **
         **                                                             **
         *****************************************************************
         *****************************************************************

                           **** MACROS  DEFINITIONS ****

         CJP    MAC   JC,JA              CONDITIONAL JUMP-IF 'JC' GO TO 'JA'
                VFD   N1/0,X6/'JC',X9/'JA'-START1
                EMC
         UJP    MAC   JA                      UNCONDITIONAL JUMP-GO TO 'JA'
                VFD   N7/0,X9/'JA'-START1
                EMC
         LDC    MAC   D,C                     LOAD CONSTANT-LOAD 'D' BY 'C'
                VFD   N4/$8,X4/'D',X8/'C'
                EMC
         LADDR  MAC   D,AD                    LOAD ADDRESS-LOAD 'D' BY
         *                                         VALUE OF LABEL 'AD'
                VFD   N4/$8,X4/'D',X8/'AD'-START1
                EMC
         SFFCL  MAC   FF,CL                   SET FLIP FLOP & CONTROL LINE
         *                               SET 'FF' & PROVIDE  PULSE ON 'CL'
                VFD   N4/$B,X4/'CL',N2/0,X6/'FF'
                EMC
```

```
        RFFCL   MAC     FF,CL                   RESET FLIP FLOP & CONTROL LINE
        *                               RESET 'FF' & PROVIDE  PULSE ON 'CL'
                VFD     N4/$A,X4/'CL',N2/0,X6/'FF'
                EMC
        CLO     MAC     CL                        CONTROL LINE (ONLY)-
        *                                               PROVIDE  PULSE ON 'CL'
                VFD     N4/$B,X4/'CL',N8/$FF
                EMC
        SFF     MAC     FF                        SET FLIP FLOP-SET 'FF'
                VFD     N10/$2FC,X6/'FF'
                EMC
        RFF     MAC     FF                        RESET FLIP FLOP-RESET 'FF'
                VFD     N10/$2BC,X6/'FF'
                EMC
        *
        *
        *
        *                             ** INTER REGISTER LOGICAL FUNCTIONS **
        *
        *
        *
        TA      MAC     SA,D                      TRANSFER A:    SA--->D
                VFD     N4/$C,X4/'D',N5/$1E,X3/'SA'
                EMC
        CA      MAC     SA,D                      COMPLEMENT A:    SA/--->D
                VFD     N4/$C,X4/'D',N5/$0,X3/'SA'
                EMC
        TB      MAC     SB,D                      TRANSFER B:     SB--->D
                VFD     N2/$3,X2/'SB',X4/'D',N8/$A0
                EMC
        CB      MAC     SB,D                      COMPLEMENT B:   SB/--->D
                VFD     N2/$3,X2/'SB',X4/'D',N8/$50
                EMC
        CLEAR   MAC     D                         CLEAR      :    00--->D
                VFD     N4/$F,X4/'D',N8/$35
                EMC
        SETONE  MAC     D                         SET TO ONE:    FF--->D
                VFD     N4/$F,X4/'D',N8/$C5
                EMC
```

```
         OR       MAC    SA,SB,D                    OR:    SA.OR.SB--->D
                  VFD    N2/$3,X2/'SB',X4/'D',N5/$1C,X3/'SA'
                  EMC
         COR      MAC    SA,SB,D         COMPLEMENT OR (NOR):(SA.OR.SB)/--->D
                  VFD    N2/$3,X2/'SB',X4/'D',N5/$2,X3/'SA'
                  EMC
         ORCA     MAC    SA,SB,D              OR COMPLEMENT B: SA.OR.(SB/)--->D
                  VFD    N2/$3,X2/'SB',X4/'D',N5/$10,X3/'SA'
                  EMC
         ORCB     MAC    SA,SB,D            OR COMPLEMENT A: (SA/).OR.SB--->D
                  VFD    N2/$3,X2/'SB',X4/'D',N5/$1A,X3/'SA'
                  EMC
         XOR      MAC    SA,SB,D                    EXCLUSIVE OR:  SA.XOR.SB--->D
                  VFD    N2/$3,X2/'SB',X4/'D',N5/$C,X3/'SA'
                  EMC
         CXOR     MAC    SA,SB,D                    COMPLEMENT EXCLUSIVE OR:
         *                                                    (SA.XOR.SB)/--->D
                  VFD    N2/$3,X2/'SB',X4/'D',N5/$12,X3/'SA'
                  EMC
         ANDAB    MAC    SA,SB,D                    AND A B:   SA.AND.SB--->D
                  VFD    N2/$3,X2/'SB',X4/'D',N5/$16,X3/'SA'
                  EMC
         CAND     MAC    SA,SB,D                    COMPLEMENT AND (NAND):
         *                                                    (SA.AND.SB)/--->D
                  VFD    N2/$3,X2/'SB',X4/'D',N5/$B,X3/'SA'
                  EMC
         ANDCA    MAC    SA,SB,D          AND COMPLEMENT A: (SA/).AND.SB--->D
                  VFD    N2/$3,X2/'SB',X4/'D',N5/$4,X3/'SA'
                  EMC
         ANDCB    MAC    SA,SB,D                    AND COMPLEMENT B:
         *                                               SA.AND.(SB/)--->D
                  VFD    N2/$3,X2/'SB',X4/'D',N5/$E,X3/'SA'
                  EMC
```

```
         *                                ** INTER REGISTER ARITHMETIC OPERATIONS **
         *
         *
         *
         *                                         FLIP-FLOP CN SHOULD
         *                                         BE PROPERLY SET OR RESET
         *                                        BEFORE AN ARITHMETIC OPERATION
         *                                         IS EXECUTED.
         *
         *
         IA       MAC      SA,D                    INCREMENT A:  SA+1--->D
         *                                         CONDITION  CN=1
                  VFD      N4/$C,X4/'D',N5/$1,X3/'SA'
                  EMC
         DA       MAC      SA,D                    DECREMENT A:  SA-1--->D
         *                                         CONDITION  CN=1
                  VFD      N4/$C,X4/'D',N5/$1F,X3/'SA'
                  EMC
         PLUS     MAC      SA,SB,D                 PLUS:   SA+SB--->D
         *                                         CONDITION  CN=0
                  VFD      N2/$3,X2/'SB',X4/'D',N5/$13,X3/'SA'
                  EMC
         MINUS    MAC      SA,SB,D                 MINUS:  SA-SB--->D
         *                                         CONDITION  CN=1
                  VFD      N2/$3,X2/'SB',X4/'D',N5/$D,X3/'SA'
                  EMC
         PLUSI    MAC      SA,SB,D                 PLUS INCREMENT:  SA+SB+1--->D
         *                                         CONDITION  CN=1
                  VFD      N2/$3,X2/'SB',X4/'D',N5/$13,X3/'SA'
                  EMC
         LSFT     MAC      SA,D                    LEFT SHIFT:   SA+SA--->D
         *                                         CONDITION  CN=0
                  VFD      N4/$C,X4/'D',N5/$19,X3/'SA'
                  EMC
         LSFTI    MAC      SA,D              LEFT SHIFT INCREMENT: SA+SA+1--->D
         *                                         CONDITION  CN=1
                  VFD      N4/$C,X4/'D',N5/$19,X3/'SA'
                  EMC
```

```
          COMPR   MAC     SA,SB                     COMPR:     SA=SB ?
          *                                         CONDITION   CN=1
          *                                         THE RESULT IS SENSED ON THE
          *                                  A=B PIN OF THE ALU. THE DESTINATION
          *                                         IS AN UNUSED REGISTER;
          *                                         THEREFORE DATA REMAINS
          *.                                        UNCHANGED
                  VFD     N2/$3,X2/'SB',N9/$6D,X3/'SA'
                  EMC
          *
          *
          *
          IRAR    MAC     M,SA,SB,D           INTER REGISTER ARITHMETIC (GENERAL)
          *                                     THIS INSTRUCTION COVERS  ALL 16
          *                                         AVAILABLE MODES OF ARITHMETIC
          *                                         OPERATIONS. ALL 16 MODES
          *                                         DEPEND ON THE STATE OF
          *                                         THE CN FLIP-FLOP.
          *                                         REFFER TO IRAR MODE DEF.
          *
          *                                         'M' IS THE MODE SYMBOL
          *
                  VFD     N2/$3,X2/'SB',X4/'D',X4/'M',N1/$1,X3/'SA'
                  EMC
          *
          NOOP    MAC
          *                                         NO OPERATION
          *
                  VFD     N16/$BFFF
                  EMC
          SPARE   MAC
          *                                         SPARE-
          *                            PROM WORD REMAINS UNBURNED
                  VFD     N16/$FFFF
                  EMC
```

```
          *                                       **** IRAR  MODE DEFINITIONS ****

0000            EQU     MODE0($0)                 MODE0: SA+/+CN--->D
0001            EQU     MODE1($1)                 MODE1: (SA.OR.SB)+CN--->D
0002            EQU     MODE2($2)                 MODE2: (SA.OR.(SB/))+CN--->D
0003            EQU     MODE3($3)                 MODE3: FFFF+CN--->D
0004            EQU     MODE4($4)              MODE4: SA+(SA.AND.(SB/))+CN--->D
0005            EQU     MODE5($5)                 MODE5:
          *                                    (SA.OR.SB)+(SA.AND.(SB/)+CN--->D
0006            EQU     MODE6($6)                 MODE6: SA-SB-1+CN--->D
0007            EQU     MODE7($7)               MODE7: (SA.AND.(SB/)-1+CN--->D
0008            EQU     MODE8($8)                 MODE8: SA+(SA.AND.SB)+CN--->D
0009            EQU     MODE9($9)                 MODE9: SA+SB+CN--->D
000A            EQU     MODEA($A)                 MODEA:
          *                                   (SA.OR.(SB/))+(SA.AND.SB)+CN--->D
000B            EQU     MODEB($B)                 MODEB:(SA.AND.SB)-1+CN--->D
000C            EQU     MODEC($C)                 MODEC: SA+SA+CN--->D
000D            EQU     MODED($D)                 MODED: (SA.AND.SB)+SA+CN--->D
000E            EQU     MODEE($E)              MODEE: (SA.AND.(SB/))+SA+CN--->D
000F            EQU     MODEF($F)                 MODEF: SA-1+CN--->D

          *                                       **** DESTINATION REGISTERS ****

0003            EQU     NU($3)                    NOT USED
0004            EQU     RAMADD($4)                RAM ADDRESS
0005            EQU     BANKD($5)                 COMPUTER MEMOY BANK
0006            EQU     RAMD($6)                  RAM
0007            EQU     PCD($7)                   PROGRAM COUNTER
0008            EQU     WCD($8)                   WORD COUNTER
0009            EQU     AOUTUD($9)                A REGISTER OUT UPPER BYTE
000A            EQU     CWALD($A)                 CURRENT WORD ADDRESS-
          *                                                   LOWER BYTE
000B            EQU     CWAUD($B)                 CURRENT WORD ADDRESS-
          *                                                   UPPER BYTE
000C            EQU     AOUTLD($C)                A REGISTER OUT LOWER BYTE
000D            EQU     BF2LD($D)                 BUFFER 2 LOWER BYTE
000E            EQU     BF2UD($E)                 BUFFER 2 UPPER BYTE
000F            EQU     BREGD($F)                 B REGISTER
```

```
                 *                                   **** SOURCE A REGISTERS ****

        0000           EQU    RAMS($0)                   RAM
        0001           EQU    WCS($1)                    WORD COUNTER
        0002           EQU    AINLS($2)                  A LINES IN LOWER BYTE
        0003           EQU    AINUS($3)                  A LINES IN UPPER BYTE
        0004           EQU    BREGS($4)                  B REGISTER
        0005           EQU    QS($5)                     Q LINES
        0007           EQU    PCS($7)                    PROGRAM COUNTER

                 *                                   **** SOURCE B REGISTERS ****

        0000           EQU    CWALS($0)                  COURENT WORD ADDRESS-
                 *                                                   LOWER BYTE
        0001           EQU    CWAUS($1)                  COURENT WORD ADDRESS-
                 *                                                   UPPER BYTE
        0002           EQU    BF2LS($2)                  BUFFER 2 LOWER BYTE
        0003           EQU    BF2US($3)                  BUFFER 2 UPPER BYTE

                 *                                   **** CONTROL LINES ****

        0001           EQU    REJ($1)                    SET REJECT
        0002           EQU    DMAREQ($2)                 SET DMA REQUEST
        0003           EQU    RPLY($3)                   SET REPLY
        0004           EQU    CRCERCL($4)                CRC ERROR CIRCUIT
                 *                                                 ENABLE (CL)
        0005           EQU    CREQ($5)                   CLEAR DMA REQUST
        0006           EQU    FRINXCL($6)                SET FORCE RELEASE INDEX (CL)
        0007           EQU    RDZERO($7)                 READ ZEROES-
                 *                                       ENABLE SEARCH FIRST OF DATA
        0008           EQU    SBF1F($8)                  SET BUFFER 1 FULL
        0009           EQU    SBF2F($9)                  SET BUFFER 2 FULL
        000A           EQU    CBITC($A)                  CLEAR BIT COUNTER
        000B           EQU    CNET($B)                   CLEAR NETWORK
        000D           EQU    CDMAER($D)                 CLEAR DMA ERROR
        000E           EQU    CWORD($E)                  CLEAR WORD
```

```
                *                        **** JUMP CONDITIONS ****
                *                              JUMP CONDITION GROUPS
                *                              1 AND 9 HAVE THE SAME
                *                              BIT CONFIGURATIONS.
                *                              SELECTION BETWEEN GROUPS
                *                              IS PERFORMED BY SETTING
                *                              OR RESETTING JGRP9 FLIP-FLOP
                *
0003                EQU   ADRERR($03)    JC46  DMA ADDRESS ERROR
002A                EQU   ALARMJC($2A)   JC62  ALARM (JC)
003E                EQU   ALDFXD($3E)    JC50  AUTOLOAD FIXED DISK
000E                EQU   ALDENJC($0E)   JC10  AUTOLOAD & ENPRTSYS (JC)
0027                EQU   AUTOLD($27)    JC24  AUTOLOAD PUSH BUTTON
002E                EQU   ALTFRC($2E)    JC60  ALTERNATE FORCE
0012                EQU   AUXJC($12)     JC86  AUXILIARY (JC)
0019                EQU   BF1F($19)      JC33  BUFFER 1 FULL
0007                EQU   BF2F($07)      JC44  BUFFER 2 FULL
0008                EQU   BLZROJC($08)   JC13  BLOCK LENGTH ZERO (JC)
001C                EQU   BL1JC($1C)     JC81  BLOCK LENGTH BIT 2**1 (JC)
0014                EQU   BMDL($14)      JC85  B REGISTER BIT 2**5
0028                EQU   BMSB($28)      JC63  B REGISTER BIT 2**7
002F                EQU   BUSBSY($2F)    JC20  BUS BUSY
0010                EQU   COMPJC($10)    JC87  COMPARE (JC)
000D                EQU   COUT($0D)      JC41  ALU CARRY OUT (COMP)
002D                EQU   CRCERJC($2D)   JC21  CRC ERROR (JC)
001B                EQU   CWAUL($1B)     JC32  CURRENT WORD ADDRESS-
                *                                              BIT 2**16
0017                EQU   CWAUM($17)     JC34  CURRENT WORD ADDRESS-
                *                                              BIT 2**17
0036                EQU   DKWTPT($36)    JC54  DISK WRITE PROTECT
002C                EQU   DSKERR($2C)    JC61  DISK ERROR
000F                EQU   EQUAL($0F)     JC40  ALU A=B
0029                EQU   FRINXJC($29)   JC23  FORCE RELEASE INDEX (JC)
0013                EQU   FRSTDT($13)    JC36  FIRST OF DATA (COMP)
001D                EQU   HFWRD($1D)     JC31  HALF WORD
002B                EQU   INDEX($2B)     JC22  INDEX
001F                EQU   LSTDT($1F)     JC30  LOST DATA
0004                EQU   MSW1($04)      JC95  MAINTENANCE SWITCH 1
000A                EQU   MSW2($0A)      JC92  MAINTENANCE SWITCH 2
0002                EQU   NOCOMP($02)    JC96  NO COMPARE
```

```
0366     001E     EQU    ONBUSJC($1E)    JC80   ON BUS (JC) (COMP)
0367     003C     EQU    ONCYL($3C)      JC51   ON CYLINDER
0368     0023     EQU    ONOFLN($23)     JC26   ON/OFF LINE SWITCH
0369     0005     EQU    PARERR($05)     JC45   DMA PARITY ERROR
0370     000B     EQU    PRTFLT($0B)     JC42   DMA PROTECT FAULT
0371     0006     EQU    PRGPRT($06)     JC14   PROGRAM PROTECT
0372     0004     EQU    RMEXEC($04)     JC15   ROM EXEC
0373     0002     EQU    SEEKER($02)     JC16   SEEK ERROR
0374     0033     EQU    SECTOR($33)     JC76   SECTOR
0375     0020     EQU    SNGDNJC($20)    JC67   SINGLE DENSITY (JC)
0376     003D     EQU    SKCMP0($3D)     JC71   SEEK COMPLETE 0
0377     003B     EQU    SKCMP1($3B)     JC72   SEEK COMPLETE 1
0378     0037     EQU    SKCMP2($37)     JC74   SEEK COMPLETE 2
0379     0035     EQU    SKCMP3($35)     JC75   SEEK COMPLETE 3
0380     000A     EQU    SNSWDJC($0A)    JC12   SENSE/WRITE ADDRESS (JC)
0381     003A     EQU    UNRDY($3A)      JC52   UNIT READY
0382     0024     EQU    UNTPRT($24)     JC65   UNIT PROTECT
0383     0006     EQU    USNGDN($06)     JC94   UNIT SINGLE DENSITY
0384     0018     EQU    WCEMPT($18)     JC83   WORD COUNTER EMPTY (COMP)
0385     0015     EQU    WORD($15)       JC35   WORD (COMP)
0386     000C     EQU    WTOP1JC($0C)    JC11   WRITE OPERATION 1 (JC)
0387     0026     EQU    WTOP2JC($26)    JC64   WRITE OPERATION 2 (JC)


0389              *                      **** FLIP-FLOPS ****

0391     002F     EQU    ALARMFF($2F)    FF40   ALARM (FF)
0392     000C     EQU    ALDENFF($0C)    FF53   AUTOLOAD & ENPRTSYS (FF)
0393     0034     EQU    AUXFF($34)      FF13   AUXILIARY (FF)
0394     001E     EQU    BF1ENB($1E)     FF31   BUFFER 1 ENABLE
0395     000A     EQU    BLZROFF($0A)    FF55   BLOCK LENGTH ZERO (FF)
0396     0032     EQU    BL1FF($32)      FF15   BLOCK LENGTH BIT 2**1 (FF)
0397     002E     EQU    BUSY($2E)       FF41   CONTROLLER BUSY
0398     0031     EQU    CABIT0($31)     FF16   CYLINDER ADDRESS BIT 2**0
0399     0036     EQU    CASTRB($36)     FF11   CYLINDER ADDRESS STROBE
0400     0020     EQU    CNALU($20)      FF67   ALU CN (CARRY IN)
0401     0000     EQU    CNTPRT($00)     FF77   CONTROLLER PROTECT
0402     0030     EQU    COMPFF($30)     FF17   COMPARE (FF)
```

```
001A   EQU   COMP1($1A)     FF35   COMPARE 1
000E   EQU   COMP2($0E)     FF51   COMPARE 2
002B   EQU   CRCMOD($2B)    FF44   CRC MODE
0018   EQU   CSFTRG($18)    FF37   CLEAR SHIFT REGISTER
002C   EQU   DMWRPT($2C)    FF43   DMA WRITE PROTECT
001C   EQU   EGWG($1C)      FF33   ERASE GATE & WRITE GATE
001D   EQU   ENBDB($1D)     FF32   ENABLE DOUBLE BUFFER
000B   EQU   ENBNED($0B)    FF54   ENABLE NEED
001B   EQU   ENWDSY($1B)    FF34   ENABLE WORD SYNC
0003   EQU   EOP($03)       FF74   END OF OPERATION
002A   EQU   FRCBUS($2A)    FF45   FORCED BUS
000D   EQU   HS1($0D)       FF52   HEAD SELECT 1 (SURFACE)
0013   EQU   HS2($13)       FF24   HEAD SELECT 2 (DISK)
0028   EQU   INTRSP($28)    FF47   INTERUPT RESPONSE
0029   EQU   JGRP9($29)     FF46   JUMP CONDITIONS GROUP 9 ENB
0023   EQU   ONBUSFF($23)   FF64   ON BUS (FF)
0007   EQU   PRIOR($07)     FF70   PRIORITY
0011   EQU   RDGATE($11)    FF26   READ GATE
0033   EQU   RMBNKS($33)    FF14   ROM BANK SELECT
0022   EQU   RQBUS1($22)    FF65   REQUEST BUS 1
000F   EQU   RQBUS2($0F)    FF50   REQUEST BUS 2
0014   EQU   RTZS($14)      FF23   RTZS
0019   EQU   RWMOD($19)     FF36   READ/WRITE MODE
0017   EQU   SELBF1($17)    FF20   SELECT BUFFER 1
0010   EQU   SELBF2($10)    FF27   SELECT BUFFER 2
0002   EQU   SNGDNFF($02)   FF75   SINGLE DENSITY (FF)
0008   EQU   SNSWDFF($08)   FF57   SENSE/WRITE ADDRESS (FF)
0037   EQU   TRKOFS($37)    FF10   TRACK OFFSET
0021   EQU   US0($21)       FF66   UNIT SELECT 0
0026   EQU   US1($26)       FF61   UNIT SELECT 1
0025   EQU   US2($25)       FF62   UNIT SELECT 2
0024   EQU   US3($24)       FF63   UNIT SELECT 3
0009   EQU   WTOP1FF($09)   FF56   WRITE OPERATION 1 (FF)
0006   EQU   WTOP2FF($06)   FF71   WRITE OPERATION 2 (FF)
001F   EQU   WTRDMP($1F)    FF30   WRITE/READ MP

       ENT   START1
```

```
                   ******************************************************************
                   *                                                                *
                   *                      *** START ***                             *
                   *                                                                *
                   *        DETERMINES THE REASONS FOR PROGRAM COUNTER RESET:       *
                   *        1. MASTER CLEAR                                         *
                   *        2. CLEAR CONTROLLER                                     *
                   *        3. FORCED BUS RELEASE                                   *
                   *                                                                *
                   ******************************************************************

                   START1 UJP    START2
     P0000 0001
                   START2 CJP    ALTFRC,RTZS13
     P0001 5C2C
                          LDC    RAMADD,4
     P0002 8404
                          LDC    RAMD,$0
     P0003 8600
                          UJP    WL20
     P0004 0055

                   ******************************************************************
                   *                                                                *
                   *    *** MEMORY BANK SELECT AND LOAD FILE ADDRESS COMMANDS ***   *
                   *                                                                *
                   ******************************************************************

                   BANK   CA     AINUS,BANKD     MEMORY BANK SELECT COMMAND
     P0005 C503
                   FILEAD CA     AINLS,BREGD     LOAD FILE ADDRES COMMAND
     P0006 CF02
                          UJP    REPLY
     P0007 011C
```

```
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0470                   *************************************************************
0471                   *                                                           *
0472                   *            *** DIRECTOR FUNCTION DECODE ***               *
0473                   *                         DIRECTOR FUNCTION A LINES DECODE :  *
0474                   *                                                           *
0475                   *************************************************************

0477                        UJP    WLBU1
0477 P0008 0000
0478                        UJP    READ2                  READ FUNCTION
0478 P0009 00CB
0479                        UJP    WRT16                  WRITE FUNCTION
0479 P000A 012E
0480                        UJP    WRT14                  COMPARE FUNCTION
0480 P000B 012C
0481                        UJP    READ1                  CHECK-WORD-CHECK FUNCTION
0481 P000C 00CA
0482                        UJP    WAD1                   WRITE ADDRESS FUNCTION
0482 P000D 0098
0483                        UJP    SSS1                   SENSE VERIFY FUNCTION
0483 P000E 0014
0484                        UJP    WLBU1
0484 P000F 0000

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0486                   *************************************************************
0487                   *                                                           *
0488                   *             *** INPUT INSTRUCTION DECODE ***              *
0489                   *                                                           *
0490                   *                                  Q LINES DECODE:          *
0491                   *                                                           *
0492                   *************************************************************

0494                        UJP    REJECT
0494 P0010 007A
0495                        UJP    REPLY                  A OUT STATUS
0495 P0011 011C
0496                        UJP    CWAS1                  CWA STATUS
0496 P0012 0087
0497                        UJP    BSS1                   BANK SELECT STATUS
0497 P0013 0016
0498                        UJP    RDFL1                  FILE STATUS
0498 P0014 0082
0499                        UJP    SCS2                   SEEK COMPLETE STATUS
0499 P0015 010F
```

```
                   ****************************************************************
                   *                                                              *
                   *            *** MEMORY BANK SELECT STATUS COMMAND ***         *
                   *                                                              *
                   ****************************************************************

                   BSS1   LDC    AOUTUD,$C0
     P0016 89C0
                          CJP    CWAUL,BSS8
     P0017 361D
                          CJP    CWAUM,BSS6
     P0018 2E1B
                          LDC    AOUTUD,$0
     P0019 8900
                          UJP    REPLY
     P001A 011C
                   BSS6   LDC    AOUTUD,$80
     P001B 8980
                          UJP    REPLY
     P001C 011C
                   BSS8   CJP    CWAUM,REPLY
     P001D 2F1C
                          LDC    AOUTUD,$40
     P001E 8940
                          UJP    REPLY
     P001F 011C


                   ****************************************************************
                   *                                                              *
                   *                    ***  RTZS COMMAND  ***                    *
                   *                                                              *
                   ****************************************************************

                   RTZS1  SFF    RTZS
     P0020 8F14
```

```
                          RFF    ALARMFF
P0021 AF2F
                          IRAR   MODEF,PCS,BF2US,NU
P0022 F3FF
                          RFF    RTZS
P0023 AF14
                          LDC    BF2LD,$F6
P0024 8DF6
                          CJP    ALDENJC,RTZS8
P0025 1C27
                          CJP    ONOFLN,REPLY
P0026 471C
                  RTZS8   CJP    ONCYL,ATLD23
P0027 7992
                          CJP    SEEKER,RTZS1
P0028 0420
                          UJP    RTZS8
P0029 0027
                          SPARE
P002A FFFF
                          SPARE
P002B FFFF


                  ***********************************************************************
                  *                                                                     *
                  *                    *** BUS RELINQUISH STATUS ***                    *
                  *                                                                     *
                  ***********************************************************************

                  RTZS13  SFFCL  ALARMFF,FRINXCL
P002C B62F
                          LDC    RAMADD,$6
P002D 8406
                          LDC    RAMD,$0
P002E 8600
                          UJP    WL20
P002F 0055
```

```
0549                    ******************************************************************
0550                    *                                                                *
0551                    *                 *** OUTPUT INSTRUCTION DECODE ***              *
0552                    *                                                                *
0553                    *                              DECODE Q LINES:                   *
0554                    *                                                                *
0555                    ******************************************************************

0557                          UJP    REJECT
0557 P0030 007A
0558                          UJP    DF1                DIRECTOR FUNCTION
0558 P0031 00E0
0559                          UJP    FWAD1              FIRST WORD ADDRESS
0559 P0032 00B5
0560                          UJP    BANK               BANK SELECT
0560 P0033 0005
0561                          UJP    FILEAD             LOAD FILE ADDRESS
0561 P0034 0006
0562                          UJP    WFSC1              WAIT FOR SEEK CHANGE
0562 P0035 011E
0563                          UJP    US01               UNIT SELECT
0563 P0036 0127
0564                          UJP    LDBL1              LOAD BLOCK LENGTH
0564 P0037 008A
0565                          UJP    BSCN1              BUS CONNECT
0565 P0038 0099
0566                          UJP    INRQ1              INTERRUPT REQUEST
0566 P0039 008F
0567                          UJP    STD1               SEEK TO DEVICE
0567 P003A 00B8
0568                          UJP    LDAD1              LOAD DISK ADDRESS
0568 P003B 007D
0569                          UJP    TST11              SELF TEST1
0569 P003C 014C
0570                          UJP    TST21              SELF TEST2
0570 P003D 01B7
0571                          UJP    TST31              SELF TEST3
0571 P003E 0164
0572                          UJP    TST41              SELF TEST4
0572 P003F 015F
```

```
0575                  ****************************************************************
0576                  *                                                              *
0577                  *     *** WAITING LOOP AND TERMINATION OF BUSY ROUTINES ****   *
0578                  *                                                              *
0579                  *     THIS ROUTINE TERMINATE ALL BUSY ROUTINES.                *
0580                  *     FIRST IT INITIALISES FF'S AND REGISTERS IN PREPARATION   *
0581                  *     FOR THE NEXT OPERATION.                                  *
0582                  *      NEXT THIS LOOP CONTINUOUSLY SAMPLES: ROM EXEC FF,AUTOLOAD*
0583                  *     SIGNAL AND ON/OFF LINE SWITCH TO DETERMINE THE NEXT      *
0584                  *     DESIRED OPERATION.                                       *
0585                  *                                                              *
0586                  ****************************************************************

0588                  WL1     LDC     RAMADD,$6
0588 P0040 8406
0589                          CJP     ADRERR,WL4
0589 P0041 0643
0590                          UJP     WL6
0590 P0042 0045
0591                  WL4     LDC     BF2LD,$01
0591 P0043 8D01
0592                          OR      RAMS,BF2LS,RAMD
0592 P0044 E6E0
0593                  WL6     CJP     PARERR,WL8
0593 P0045 0A47
0594                          UJP     WL10
0594 P0046 0049
0595                  WL8     LDC     BF2LD,$4
0595 P0047 8D04
0596                          OR      RAMS,BF2LS,RAMD
0596 P0048 E6E0
0597                  WL10    CJP     LSTDT,WL12
0597 P0049 3E4B
0598                          UJP     WL14
0598 P004A 004D
0599                  WL12    LDC     BF2LD,$08
0599 P004B 8D08
0600                          OR      RAMS,BF2LS,RAMD
0600 P004C E6E0
```

```
0602                WL14   RFF    WTOP1FF
0602 P004D AF09
0603                       RFF    COMPFF
0603 P004E AF30
0604                       RFF    ALDENFF
0604 P004F AF0C
0605                       RFF    AUXFF
0605 P0050 AF34
0606                       RFF    ENWDSY
0606 P0051 AF1B
0607                       RFF    ENBDB
0607 P0052 AF1D
0608                       RFF    SELBF2
0608 P0053 AF10
0609                       RFF    SNSWDFF
0609 P0054 AF08
0610                WL20   SFF    BF1ENB
0610 P0055 BF1E
0611                       SFF    CNALU
0611 P0056 BF20
0612                       LDC    WCD,$10
0612 P0057 8810
0613                       LDC    BF2UD,$01
0613 P0058 8E01
0614                WL24   LDC    RAMADD,$4
0614 P0059 8404
0615                       LSFT   RAMS,BREGD
0615 P005A CFC8
0616                       CJP    FRINXJC,WL30
0616 P005B 525F
0617                       CJP    BMSB,WL34
0617 P005C 5063
0618                WL28   CJP    ALARMJC,WL32
0618 P005D 5461
0619                       UJP    WL36
0619 P005E 0065
0620                WL30   LDC    RAMADD,$7
0620 P005F 8407
0621                       LDC    RAMD,$20
0621 P0060 8620
```

```
0623                  WL32   CJP    BMDL,WL34
0623 P0061 2863
0624                         UJP    WL36
0624 P0062 0065
0625                  WL34   SFF    INTRSP
0625 P0063 BF28
0626                         CJP    FRINXJC,WL37
0626 P0064 5266
0627                  WL36   CJP    RMEXEC,REPLY
0627 P0065 091C
0628                  WL37   RFF    BUSY
0628 P0066 AF2E
0629                         SFFCL  EOP,CRCERCL
0629 P0067 B403
0630                  WL39   CJP    RMEXEC,WL53
0630 P0068 0877
0631                         CJP    ONBUSJC,WL42
0631 P0069 3C6B
0632                         CJP    BUSBSY,WL46
0632 P006A 5E70
0633                  WL42   CJP    RMEXEC,WL53
0633 P006B 0877
0634                         CJP    AUTOLD,WL45
0634 P006C 4E6E
0635                         UJP    ATLD1
0635 P006D 017D
0636                  WL45   CJP    ONOFLN,WL39
0636 P006E 4668
0637                         UJP    ATLD7
0637 P006F 0182
0638                  WL46   CJP    RMEXEC,WL53          ALTERNATE INTERRUPT REQUEST
0638 P0070 0877
0639                         LDC    RAMADD,$4
0639 P0071 8404
0640                         LSFT   RAMS,NU
0640 P0072 C3C8
0641                         CJP    RMEXEC,WL53
0641 P0073 0877
```

```
0643                    CJP    COUT,WL42
0643 P0074 1A6B
0644                    SFF    INTRSP
0644 P0075 BF28
0645                    UJP    WL42
0645 P0076 006B
0646             WL53   TA     QS,BF2LD            SAMPLES TWICE THE Q LINES
0646 P0077 CDF5
0647                    COMPR  QS,BF2LS
0647 P0078 E36D
0648                    CJP    EQUAL,WL58
0648 P0079 1E7C
0649             REJECT CLO    REJ
0649 P007A B1FF
0650                    UJP    WL39
0650 P007B 0068
0651             WL58   ORCB   WCS,BF2LS,PCD
0651 P007C E7D1


0653             ***************************************************************
0654             *                                                             *
0655             *              *** LOAD DISK ADDRESS COMMAND ***              *
0656             *                                                             *
0657             ***************************************************************


0659             LDAD1  LDC    RAMADD,$2
0659 P007D 8402
0660                    CA     AINLS,RAMD
0660 P007E C602
0661                    LDC    RAMADD,$3
0661 P007F 8403
0662                    CA     AINUS,RAMD
0662 P0080 C603
0663                    UJP    REPLY
0663 P0081 011C
```

```
                    ****************************************************************
                    *                                                              *
                    *                *** FILE STATUS COMMAND ***                   *
                    *                                                              *
                    ****************************************************************


                    RDFL1   TA      BREGS,RAMADD
     P0082 C4F4
                            TA      RAMS,AOUTLD
     P0083 CCF0
                            PLUS    BREGS,BF2US,RAMADD
     P0084 F49C
                            TA      RAMS,AOUTUD
     P0085 C9F0
                            UJP     REPLY
     P0086 011C


                    ****************************************************************
                    *                                                              *
                    *            *** CURRENT WORD STATUS COMMAND ***               *
                    *                                                              *
                    ****************************************************************


                    CWAS1   TB      CWALS,AOUTLD
     P0087 CCA0
                            TB      CWAUS,AOUTUD
     P0088 D9A0
                            UJP     REPLY
     P0089 011C
```

```
0687                   ****************************************************************
0688                   *                                                              *
0689                   *              *** LOAD BLOCK LENGTH COMMAND ***               *
0690                   *                                                              *
0691                   ****************************************************************


0693                   LDBL1  LDC    RAMADD,$8
0693 P008A 8408
0694                          CA     AINLS,RAMD
0694 P008B C602
0695                          LDC    RAMADD,$9
0695 P008C 8409
0696                          CA     AINUS,RAMD
0696 P008D C603
0697                          UJP    REPLY
0697 P008E 011C


0699                   ****************************************************************
0700                   *                                                              *
0701                   *              *** INTERRUPT REQUEST COMMAND ***               *
0702                   *                                                              *
0703                   ****************************************************************


0705                   INRQ1  LDC    RAMADD,$4
0705 P008F 8404
0706                          CA     AINLS,BREGD
0706 P0090 CF02
0707                          CJP    BMSB,INRQ7
0707 P0091 5095
0708                          LSFT   BREGS,BF2LD
0708 P0092 CDCC
0709                          OR     RAMS,BF2LS,RAMD
0709 P0093 E6E0
```

```
                          UJP     INRQ9
P0094  0097
                  INRQ7   LSFT    BREGS,RAMD
P0095  C6CC
                          RFF     INTRSP
P0096  AF28
                  INRQ9   LSFT    RAMS,BREGD
P0097  CFC8
                          UJP     WL28
P0098  005D

                  *****************************************************************
                  *                                                               *
                  *                *** BUS CONNECT COMMAND ***                    *
                  *                                                               *
                  *****************************************************************

                  BSCN1   CA      AINLS,BREGD
P0099  CF02
                          CJP     BMSB,BSCN6
P009A  509E
                          RFF     RQBUS1
P009B  AF22
                          RFFCL   ONBUSFF,RPLY          RPLY   ONBUSFF
P009C  A323
                          UJP     WL20
P009D  0055
                  BSCN6   RFF     EOP
P009E  AF03
                          SFFCL   BUSY,RPLY
P009F  B32E
                          SFF     AUXFF
P00A0  BF34
                          CJP     BMDL,BSCN19
P00A1  28AB
                  BSCN10  CJP     BUSBSY,BSCN21
P00A2  5EAD
```

```
0734                      SFF    RQBUS1
0734 P00A3 BF22
0735                      SFF    RQBUS2
0735 P00A4 BF0F
0736                      NOOP
0736 P00A5 BFFF
0737                      CJP    BUSBSY,BSCN21
0737 P00A6 5EAD
0738                      RFF    RQBUS2
0738 P00A7 AF0F
0739               BSCN16 SFF    ONBUSFF
0739 P00A8 BF23
0740                      CJP    AUXJC,WL14
0740 P00A9 244D
0741                      UJP    ATLD12
0741 P00AA 0187
0742               BSCN19 SFF    FRCBUS                  FORCED RELEASED
0742 P00AB BF2A
0743                      SFF    RQBUS1
0743 P00AC BF22
0744               BSCN21 NOOP
0744 P00AD BFFF
0745                      RFF    RQBUS1
0745 P00AE AF22
0746                      NOOP
0746 P00AF BFFF
0747                      RFF    RQBUS2
0747 P00B0 AF0F
0748                      RFF    FRCBUS
0748 P00B1 AF2A
0749                      SFF    RQBUS1
0749 P00B2 BF22
0750               BSCN27 CJP    BUSBSY,BSCN27
0750 P00B3 5EB3
0751                      UJP    BSCN16
0751 P00B4 00A8
```

```
                 ******************************************************************
                 *                                                                *
                 *                 *** FIRST WORD ADDRESS COMMAND ***             *
                 *                                                                *
                 ******************************************************************


                 FWAD1   CA      AINLS,CWALD
     P00B5 CA02
                         CA      AINUS,CWAUD
     P00B6 CB03
                         UJP     REPLY
     P00B7 011C


                 ******************************************************************
                 *                                                                *
                 *                   *** SEEK TO DEVICE COMMAND ***               *
                 *                                                                *
                 ******************************************************************


                 STD1    CJP     ONBUSJC,REJECT
     P00B8 3C7A
                         CJP     UNRDY,STD4
     P00B9 74BB
                         UJP     REJECT
     P00BA 007A
                 STD4    CJP     ONCYL,STD6
     P00BB 78BD
                         UJP     REJECT
     P00BC 007A
                 STD6    LDC     RAMADD,$3
     P00BD 8403
                         CA      AINUS,RAMD
     P00BE C603
```

```
0777                          TA      RAMS,BREGD
0777 P00BF  CFF0
0778                          LDC     RAMADD,$2
0778 P00C0  8402
0779                          CA      AINLS,RAMD
0779 P00C1  C602
0780                          SFF     BUSY
0780 P00C2  BF2E
0781                          RFFCL   EOP,RPLY
0781 P00C3  A303
0782                 STD14    LSFT    BREGS,BREGD
0782 P00C4  CFCC
0783                          LSFT    BREGS,BREGD
0783 P00C5  CFCC
0784                          LSFT    BREGS,BF2UD
0784 P00C6  CECC
0785                          TA      RAMS,BREGD
0785 P00C7  CFF0
0786                          LDC     BF2LD,$7
0786 P00C8  8D07
0787                          CJP     BMSB,STD22
0787 P00C9  50CC
0788                          LDC     WCD,$3
0788 P00CA  8803
0789                          ANDAB   WCS,BF2LS,BF2LD
0789 P00CB  EDB1
0790                 STD22    CJP     BMDL,STD25
0790 P00CC  28CF
0791                          LDC     WCD,$06
0791 P00CD  8806
0792                          ANDAB   WCS,BF2LS,BF2LD
0792 P00CE  EDB1
0793                 STD25    LSFT    BREGS,BREGD
0793 P00CF  CFCC
0794                          CJP     BMSB,STD29
0794 P00D0  50D3
0795                          LDC     WCD,$05
0795 P00D1  8805
0796                          ANDAB   WCS,BF2LS,BF2LD
0796 P00D2  EDB1
```

```
                      STD29   SFF     CABITO
     P00D3 BF31
                              CJP     BMDL,STD31A
     P00D4 28D6
                              RFF     CABITO
     P00D5 AF31
                      STD31A  TB      BF2LS,BREGD
     P00D6 EFA0
                              OR      BREGS,BF2US,WCD
     P00D7 F8E4
                              SFF     CASTRB
     P00D8 BF36
                              NOOP
     P00D9 BFFF
                              NOOP
     P00DA BFFF
                              RFF     CASTRB
     P00DB AF36
                      STD38   SFF     RMBNKS
     P00DC BF33
                              CJP     AUXJC,ADV49        BRANCH POINT:ADVANCE
     P00DD 248E
                              UJP     WLBU1              SUBROUTINE OR WAITING LOOP
     P00DE 0000
                              SPARE
     P00DF FFFF


                      ****************************************************************
                      *                                                              *
                      *            *** DIRECTOR FINCTION ROUTINE ***                 *
                      *                                                              *
                      ****************************************************************


                      DF1     CJP     ONBUSJC,REJECT
     P00E0 3C7A
                              CJP     UNRDY,DF4
     P00E1 74E3
```

```
0821                        UJP    REJECT
0821 P00E2 007A
0822                 DF4    TA     AINLS,BF2LD         SAMPLES TWICE THE A LINES
0822 P00E3 CDF2
0823                        COMPR  AINLS,BF2LS
0823 P00E4 E36A
0824                        CJP    EQUAL,DF8
0824 P00E5 1EE7
0825                        UJP    REJECT
0825 P00E6 007A
0826                 DF8    CB     BF2LS,BREGD
0826 P00E7 EF50
0827                        CJP    BMDL,RTZS1
0827 P00E8 2820
0828                        RFF    DMWRPT
0828 P00E9 AF2C
0829                        CJP    PRGPRT,DF15
0829 P00EA 0CEC
0830                        SFF    DMWRPT
0830 P00EB BF2C
0831                 DF15   LDC    RAMADD,$1
0831 P00EC 8401
0832                        CA     AINUS,RAMD
0832 P00ED C603
0833                        SFF    BUSY
0833 P00EE BF2E
0834                        RFFCL  EOP,RPLY
0834 P00EF A303
0835                        SFF    TRKOFS
0835 P00F0 BF37
0836                        CJP    BMSB,DF21A
0836 P00F1 50F3
0837                        RFF    TRKOFS
0837 P00F2 AF37
0838                 DF21A  CA     RAMS,BF2UD
0838 P00F3 CE00
0839                        LDC    RAMADD,$0C
0839 P00F4 840C
```

```
0841                        XOR    RAMS,BF2US,BREGD
0841 P00F5 FF60
0842                        LSFT   BREGS,BREGD
0842 P00F6 CFCC
0843                        SFF    HS1
0843 P00F7 BF0D
0844                        CJP    COUT,DF26
0844 P00F8 1AFA
0845                        RFF    HS1
0845 P00F9 AF0D
0846              DF26      RFF    HS2
0846 P00FA AF13
0847                        CJP    BMSB,DF28A
0847 P00FB 50FD
0848                        SFF    HS2
0848 P00FC BF13
0849              DF28A     RFF    ALARMFF
0849 P00FD AF2F
0850                        RFFCL  BLZROFF,CNFT
0850 P00FE AB0A
0851                        SFFCL  RWMOD,CDMAER
0851 P00FF BD19
0852                        SFFCL  ENWDSY,CBITC
0852 P0100 BA1B
0853                        LDC    RAMADD,$6
0853 P0101 8406
0854                        LDC    RAMD,$00
0854 P0102 8600
0855                        LDC    RAMADD,$7
0855 P0103 8407
0856                        LDC    RAMD,$00
0856 P0104 8600
0857                        RFF    CNALU
0857 P0105 AF20
0858                        CJP    SEEKER,DF38
0858 P0106 0508
0859                        CJP    ONCYL,DF40
0859 P0107 790A
0860              DF38      SFF    ALARMFF
0860 P0108 BF2F
```

```
0862                             UJP    WL14
0862 P0109 004D
0863                   DF40      SFF    RMBNKS
0863 P010A BF33
0864                             LDC    WCD,$F
0864 P010B 880F
0865                             ANDCB  WCS,BF2LS,PCD
0865 P010C E771
0866                             SPARE
0866 P010D FFFF
0867                             SPARE
0867 P010E FFFF


0869                   ******************************************************************
0870                   *                                                                *
0871                   *           *** SEEK COMPLETE STATUS COMMAND ***                 *
0872                   *                                                                *
0873                   ******************************************************************


0875                   SCS2      LDC    BREGD,$0F
0875 P010F 8F0F
0876                             CJP    SKCMP1,SCS6
0876 P0110 7712
0877                             LDC    BREGD,$0D
0877 P0111 8F0D
0878                   SCS6      CJP    SKCMP0,SCS9
0878 P0112 7B14
0879                             ANDCB  BREGS,BF2US,BREGD
0879 P0113 FF74
0880                   SCS9      CJP    SKCMP2,SCS12
0880 P0114 6F17
0881                             LDC    BF2LD,$B
0881 P0115 8D0B
0882                             ANDAB  BREGS,BF2LS,BREGD
0882 P0116 EFB4
0883                   SCS12     CJP    SKCMP3,SCS15
0883 P0117 6B1A
```

```
                     LDC     BF2LD,$07
     P0118 8D07
                     ANDAB   BREGS,BF2LS,BREGD
     P0119 EFB4
              SCS15  CJP     AUXJC,WFSC7
     P011A 2524
                     TA      BREGS,AOUTLD
     P011B CCF4
              REPLY  SFFCL   EOP,RPLY
     P011C B303
                     UJP     WL39
     P011D 0068


              *****************************************************************
              *                                                               *
              *            *** WAIT FOR SEEK CHANGE COMMAND ***               *
              *                                                               *
              *****************************************************************

              WFSC1  CJP     ONBUSJC,REJECT
     P011E 3C7A
                     CA      AINLS,CWALD
     P011F CA02
                     SFF     BUSY
     P0120 BF2E
                     RFFCL   EOP,RPLY
     P0121 A303
                     SFF     AUXFF
     P0122 BF34
                     UJP     SCS2
     P0123 010F
              WFSC7  COMPR   BREGS,CWALS
     P0124 C36C
                     CJP     EQUAL,SCS2
     P0125 1F0F
                     UJP     WL14
     P0126 004D
```

```
0908                    ******************************************************************
0909                    *                                                                *
0910                    *                 *** UNIT SELECT COMMAND ***                    *
0911                    *                                                                *
0912                    ******************************************************************

0914                    US01     CJP     ONBUSJC,REJECT
0914 P0127 3C7A
0915                             TA      AINLS,BREGD
0915 P0128 CFF2
0916                             CJP     BMSB,US6
0916 P0129 512B
0917                             CJP     UNTPRT,US8
0917 P012A 492D
0918                    US6      RFF     CNTPRT
0918 P012B AF00
0919                             UJP     US10
0919 P012C 012F
0920                    US8      CJP     PRGPRT,REJECT
0920 P012D 0C7A
0921                             SFF     CNTPRT
0921 P012E BF00
0922                    US10     RFF     US0
0922 P012F AF21
0923                             RFF     US1
0923 P0130 AF26
0924                             RFF     US2
0924 P0131 AF25
0925                             RFF     US3
0925 P0132 AF24
0926                             CJP     BMSB,REPLY
0926 P0133 511C
0927                             SFF     BUSY
0927 P0134 BF2E
0928                             RFFCL   EOP,RPLY
0928 P0135 A303
0929                             SFF     JGRP9
0929 P0136 BF29
0930                             SFF     SNGDNFF
0930 P0137 BF02
```

```
0932                         CJP    USNGDN,US23E
0932 P0138 0D3A
0933                         RFF    SNGDNFF
0933 P0139 AF02
0934              US23E      RFF    JGRP9
0934 P013A AF29
0935                         LDC    RAMADD,$C
0935 P013B 840C
0936                         LDC    BF2LD,$40
0936 P013C 8D40
0937                         ANDCA  BREGS,BF2LS,RAMD
0937 P013D E624
0938                         CJP    BMDL,US34
0938 P013E 2945
0939                         LSFT   BREGS,BREGD
0939 P013F CFCC
0940                         CJP    BMDL,US32
0940 P0140 2943
0941                         SFF    US3
0941 P0141 BF24
0942                         UJP    WL24
0942 P0142 0059
0943              US32       SFF    US2
0943 P0143 BF25
0944                         UJP    WL24
0944 P0144 0059
0945              US34       LSFT   BREGS,BREGD
0945 P0145 CFCC
0946                         CJP    BMDL,US38
0946 P0146 2949
0947                         SFF    US1
0947 P0147 BF26
0948                         UJP    WL24
0948 P0148 0059
0949              US38       SFF    US0
0949 P0149 BF21
0950                         UJP    WL24
0950 P014A 0059
0951                         SPARE
0951 P014B FFFF
```

```
                  ****************************************************************
                  *                                                              *
                  *              *** SELF TEST 1 COMMAND ***                     *
                  *                                                              *
                  ****************************************************************


                  TST11  CA      AINUS,BREGD
P014C CF03
                         CA      AINUS,BF2LD
P014D CD03
                         CA      AINLS,BF2UD
P014E CE02
                         TA      AINLS,CWAUD
P014F CBF2
                         SFF     BUSY
P0150 BF2E
                         RFFCL   EOP,RPLY
P0151 A303
                         DA      BREGS,BREGD
P0152 CFFC
                         LSFT    BREGS,BREGD
P0153 CFCC
                         PLUS    BREGS,CWAUS,BREGD
P0154 DF9C
                         RFF     CNALU
P0155 AF20
                         IA      BREGS,BREGD
P0156 CF0C
                         MINUS   BREGS,BF2LS,BREGD
P0157 EF6C
                         ANDAB   BREGS,BF2US,BREGD
P0158 FFB4
                         OR      BREGS,BF2LS,AOUTLD
P0159 ECE4
                         IA      PCS,RAMD
P015A C60F
                         UJP     TDTS1                 CALL TEST 1 DATA SUBROUTINE
P015B 0170
```

```
0976                    TB    BF2US,RAMD
0976 P015C F6A0
0977             TST118 TB    BF2US,AOUTUD
0977 P015D F9A0
0978                    UJP   WL14
0978 P015E 004D


0980             **********************************************************************
0981             *                                                                    *
0982             *              *** SELF TEST 4 COMMAND ***                           *
0983             *                                                                    *
0984             **********************************************************************


0986             TST41  CA    AINLS,BF2LD
0986 P015F CD02
0987                    CA    AINUS,BF2UD
0987 P0160 CE03
0988                    CJP   PRGPRT,TST34
0988 P0161 0D68
0989                    SFF   DMWRPT
0989 P0162 BF2C
0990                    UJP   TST34
0990 P0163 0168


0992             **********************************************************************
0993             *                                                                    *
0994             *              *** SELF TEST 3 COMMAND ***                           *
0995             *                                                                    *
0996             **********************************************************************


0998             TST31  SFF   WTRDMP
0998 P0164 BF1F
0999                    SFF   COMP1
0999 P0165 BF1A
```

```
                        SFF     SELBF2
     P0166 BF10
                        SFF     SELBF1
     P0167 BF17
               TST34    SFFCL   BUSY,CNET
     P0168 BB2E
                        RFFCL   EOP,RPLY
     P0169 A303
                        SFFCL   ENBDB,DMAREQ
     P016A B21D
               TST37    CJP     BF2F,TST39
     P016B 0F6E
                        CJP     LSTDT,TST39
     P016C 3F6E
                        UJP     TST37
     P016D 016B
               TST39    TB      BF2LS,AOUTLD
     P016E ECA0
                        UJP     TST118
     P016F 015D


               *****************************************************************
               *                                                               *
               *            *** TEST 1 DATA SUBROUTINE ***                     *
               *                                                               *
               *****************************************************************

               TDTS1    LDC     BREGD,$F1
     P0170 8FF1
               TDTS2    TA      BREGS,RAMADD
     P0171 C4F4
                        TB      BF2US,CWAUD
     P0172 FBA0
                        TB      CWAUS,CWALD
     P0173 DAA0
                        TB      CWALS,WCD
     P0174 C8A0
```

```
1024                      TA     WCS,BF2LD
1024 P0175 CDF1
1025                      TB     BF2LS,RAMD
1025 P0176 E6A0
1026                      IA     RAMS,BF2UD
1026 P0177 CE08
1027                      IA     BREGS,BREGD
1027 P0178 CF0C
1028                      CJP    COUT,TDTS2
1028 P0179 1B71
1029                      LDC    RAMADD,$0
1029 P017A 8400
1030                      IA     RAMS,PCD
1030 P017B C708
1031                      SPARE
1031 P017C FFFF


1033               ****************************************************************
1034               *                                                              *
1035               *      *** AUTOLOAD AND OFFLINE PREPARATIONS ROUTINE ***       *
1036               *                                                              *
1037               ****************************************************************


1039               ATLD1  CJP    AUTOLD,WL39           ENTRY FOR AUTOLOAD
1039 P017D 4E68
1040                      CJP    ONBUSJC,ATLD4
1040 P017E 3D80
1041                      UJP    WL39
1041 P017F 0068
1042               ATLD4  SFF    DMWRPT
1042 P0180 BF2C
1043                      SFF    ALDENFF
1043 P0181 BF0C
1044               ATLD7  RFF    US1                   ENTRY FOR OFF-LINE
1044 P0182 AF26
1045                      RFF    US2
1045 P0183 AF25
```

```
1047                         RFF    US3
1047 P0184 AF24
1048                         SFF    US0
1048 P0185 BF21
1049                         UJP    BSCN10
1049 P0186 00A2
1050              ATLD12 CJP    UNRDY,RTZS1              SEARCH FOR THE FIRST UNIT
1050 P0187 7420
1051                         SFF    US1                      THAT IS READY
1051 P0188 BF26
1052                         RFF    US0
1052 P0189 AF21
1053                         CJP    UNRDY,RTZS1
1053 P018A 7420
1054                         SFF    US2
1054 P018B BF25
1055                         RFF    US1
1055 P018C AF26
1056                         CJP    UNRDY,RTZS1
1056 P018D 7420
1057                         SFF    US3
1057 P018E BF24
1058                         RFF    US2
1058 P018F AF25
1059                         CJP    UNRDY,RTZS1
1059 P0190 7420
1060                         UJP    STD38
1060 P0191 00DC
1061              ATLD23 LDC    RAMADD,$C
1061 P0192 840C
1062                         LDC    RAMD,$40
1062 P0193 8640
1063                         CJP    ALDFXD,ATLD27
1063 P0194 7D96
1064                         LDC    RAMD,$0
1064 P0195 8600
1065              ATLD27 CJP    ALDENJC,ATLD44
1065 P0196 1DA7
1066                         SFF    JGRP9        DECODE OF THE MAINTENANCE SWITCHES
1066 P0197 BF29
```

```
1068                       LDC    RAMADD,$2
1068 P0198 8402
1069                       CJP    MSW1,ATLD38
1069 P0199 09A1
1070                       LDC    BREGD,$04
1070 P019A 8F04
1071                       LDC    RAMD,$90
1071 P019B 8690
1072                       CJP    MSW2,ATLD36
1072 P019C 159F
1073                       LDC    RAMD,$20
1073 P019D 8620
1074                       LDC    BREGD,$09
1074 P019E 8F09
1075            ATLD36 RFF    JGRP9
1075 P019F AF29
1076                       UJP    STD14
1076 P01A0 00C4
1077            ATLD38 LDC    BREGD,$0
1077 P01A1 8F00
1078                       LDC    RAMD,$50
1078 P01A2 8650
1079                       CJP    MSW2,ATLD36
1079 P01A3 159F
1080                       LDC    RAMD,$A0
1080 P01A4 86A0
1081                       RFF    JGRP9
1081 P01A5 AF29
1082                       UJP    STD14
1082 P01A6 00C4
1083            ATLD44 LDC    CWAUD,$0
1083 P01A7 8B00
1084                       LDC    CWALD,$0
1084 P01A8 8A00
1085                       LDC    BANKD,$0
1085 P01A9 8500
1086                       LDC    RAMADD,$9
1086 P01AA 8409
1087                       LDC    RAMD,$0A
1087 P01AB 860A
```

```
1089                      LDC    RAMADD,$8
1089 P01AC 8408
1090                      LDC    RAMD,$E0
1090 P01AD 86E0
1091                      LDC    RAMADD,$3
1091 P01AE 8403
1092                      LDC    RAMD,$0
1092 P01AF 8600
1093                      LDC    RAMADD,$2
1093 P01B0 8402
1094                      LDC    RAMD,$0
1094 P01B1 8600
1095                      LDC    RAMADD,$1
1095 P01B2 8401
1096                      LDC    RAMD,$0
1096 P01B3 8600
1097                      UJP    DF21A
1097 P01B4 00F3
1098                      SPARE
1098 P01B5 FFFF
1099                      SPARE
1099 P01B6 FFFF


1101               ****************************************************************
1102               *                                                              *
1103               *            *** SELF TEST 2 LOWER SECTION ***                 *
1104               *                                                              *
1105               ****************************************************************


1107               TST21  RFF    ONBUSFF
1107 P01B7 AF23
1108                      SFF    BUSY
1108 P01B8 BF2E
1109                      RFFCL  EOP,RPLY
1109 P01B9 A303
```

```
1111                      RFFCL  WTOP2FF,CRCERCL
1111 P01BA A406
1112                      CJP    ALDENJC,TST258
1112 P01BB 1DF0
1113                      CJP    WTOP1JC,TST258
1113 P01BC 19F0
1114                      CJP    SNSWDJC,TST258
1114 P01BD 15F0
1115                      CJP    FRINXJC,TST258
1115 P01BE 53F0
1116                      SFFCL  CSFTRG,CDMAER
1116 P01BF BD18
1117                      SFF    ENWDSY
1117 P01C0 BF1B
1118                      SFFCL  RWMOD,CBITC
1118 P01C1 BA19
1119                      SFF    WTRDMP
1119 P01C2 BF1F
1120                      LDC    BREGD,$A5
1120 P01C3 8FA5
1121                      LDC    CWALD,$A5
1121 P01C4 8AA5
1122                      COMPR  BREGS,CWALS
1122 P01C5 C36C
1123                      CJP    HFWRD,TST258
1123 P01C6 3BF0
1124                      CJP    EQUAL,TST219
1124 P01C7 1FC9
1125                      UJP    TST258
1125 P01C8 01F0
1126               TST219 CJP    COUT,TST221
1126 P01C9 1BCB
1127                      UJP    TST258
1127 P01CA 01F0
1128               TST221 CJP    WORD,TST223
1128 P01CB 2BCD
1129                      UJP    TST258
1129 P01CC 01F0
1130               TST223 LDC    WCD,$2
1130 P01CD 8802
```

```
1132                            CJP    BMDL,TST226
1132 P01CE 29D0
1133                            UJP    TST258
1133 P01CF 01F0
1134                   TST226   CJP    BMSB,TST228
1134 P01D0 51D2
1135                            UJP    TST258
1135 P01D1 01F0
1136                   TST228   PLUS   BREGS,CWALS,BREGD
1136 P01D2 CF9C
1137                            CJP    COUT,TST258
1137 P01D3 1BF0
1138                            CJP    HFWRD,TST232
1138 P01D4 3BD6
1139                            UJP    TST258
1139 P01D5 01F0
1140                   TST232   CJP    BMDL,TST258
1140 P01D6 29F0
1141                            CJP    BMSB,TST258
1141 P01D7 51F0
1142                            PLUS   BREGS,BF2US,NU
1142 P01D8 F39C
1143                            CJP    COUT,TST237
1143 P01D9 1BDB
1144                            UJP    TST258
1144 P01DA 01F0
1145                   TST237   SFFCL  WTOP1FF,RDZERO
1145 P01DB B709
1146                            COMPR  BREGS,BF2US
1146 P01DC F36C
1147                            CJP    FRSTDT,TST241
1147 P01DD 27DF
1148                            UJP    TST258
1148 P01DE 01F0
1149                   TST241   CJP    EQUAL,TST258
1149 P01DF 1FF0
1150                            CJP    COUT,TST258
1150 P01E0 1BF0
1151                            CJP    WCEMPT,TST245
1151 P01E1 31E3
```

```
1153                        UJP    TST258
1153 P01E2 01F0
1154                 TST245 CJP    WORD,TST258
1154 P01E3 2BF0
1155                        CJP    FRSTDT,TST258
1155 P01E4 27F0
1156                        SFFCL  ENBDB,CNET
1156 P01E5 BB1D
1157                        SFFCL  ALDENFF,SBF1F
1157 P01E6 B80C
1158                        SFFCL  SNSWDFF,SBF1F
1158 P01E7 B808
1159                        CJP    BF1F,TST252
1159 P01E8 33EA
1160                        UJP    TST258
1160 P01E9 01F0
1161                 TST252 CJP    CRCERJC,TST258
1161 P01EA 5BF0
1162                        SFFCL  JGRP9,CNET
1162 P01EB BB29
1163                        CJP    NOCOMP,TST257
1163 P01EC 05EF
1164                        RFF    JGRP9
1164 P01ED AF29
1165                        CJP    BF2F,TST261
1165 P01EE 0FF3
1166                 TST257 RFF    JGRP9
1166 P01EF AF29
1167                 TST258 LDC    AOUTLD,$AD
1167 P01F0 8CAD
1168                        LDC    AOUTUD,$DE
1168 P01F1 89DE
1169                        UJP    WL14
1169 P01F2 004D
1170                 TST261 CJP    BF1F,TST258
1170 P01F3 33F0
1171                        CJP    PRTFLT,TST258
1171 P01F4 17F0
1172                        CJP    PARERR,TST258
1172 P01F5 0BF0
```

```
1174                           CJP    ADRERR,TST258
1174 P01F6 07F0
1175                           CJP    WCEMPT,TST258
1175 P01F7 31F0
1176                           SPARE
1176 P01F8 FFFF
1177                           RFFCL  SNGDNFF,CWORD
1177 P01F9 AE02
1178                           CJP    WORD,TST270
1178 P01FA 2BFC
1179                           UJP    TST258
1179 P01FB 01F0
1180                    TST270 CJP    BLZROJC,TST258
1180 P01FC 11F0
1181                           CJP    ALARMJC,TST258
1181 P01FD 55F0
1182                           SFF    RMBNKS
1182 P01FE 8F33
1183                           UJP    T2U74
1183 P01FF 01CC


1185                    ****************************************************************
1186                    *                                                              *
1187                    *                  *** WAITING LOOP UPPER SECTION ***          *
1188                    *                                                              *
1189                    ****************************************************************


1191                    WLBU1  RFF    RMBNKS                  RETURN TO THE WAITING LOOP  *
1191 P0200 AF33
1192                           CJP    ONOFLN,WL14
1192 P0201 464D
1193                           UJP    STD38
1193 P0202 00DC
```

```
1195                 ***************************************************************
1196                 *                                                             *
1197                 *        *** DECREMENT BLOCK LENGTH SUBROUTINE ***            *
1198                 *                                                             *
1199                 ***************************************************************


1201                 DCBL1   SFF     CNALU
1201 P0203 BF20
1202                         LDC     RAMADD,$8
1202 P0204 8408
1203                         DA      RAMS,RAMD
1203 P0205 C6F8
1204                         CJP     COUT,DCBL6
1204 P0206 1A08
1205                         UJP     DCBL9
1205 P0207 000B
1206                 DCBL6   LDC     RAMADD,$9
1206 P0208 8409
1207                         DA      RAMS,RAMD
1207 P0209 C6F8
1208                         CJP     COUT,DCBL12
1208 P020A 1A0E
1209                 DCBL9   RFF     CNALU
1209 P020B AF20
1210                         LDC     RAMADD,$0
1210 P020C 8400
1211                         IA      RAMS,PCD
1211 P020D C708
1212                 DCBL12  SFF     BLZROFF
1212 P020E BF0A
1213                         UJP     DCBL9
1213 P020F 000B
1214                         SPARE
1214 P0210 FFFF
1215                         SPARE
1215 P0211 FFFF
```

```
1217                     ****************************************************************
1218                     *                                                              *
1219                     *           *** SEARCH SECTOR SUBROUTINE ***                   *
1220                     *                                                              *
1221                     *        THIS SUBROUTINE SEARCHES FOR THE REQUESTED SECTOR     *
1222                     *       BY READING ADDRESS TAGS AND COMPARING THEM TO THE      *
1223                     *       REQUIRED ONE.                                          *
1224                     *        WHEN A CYLINDER MISMATCH IS DETECTED, CONTROLLER      *
1225                     *       SEEK ERROR IS DECLARED.                                *
1226                     *        IF THE REQUESTED SECTOR IS NOT FOUND WITHIN 60        *
1227                     *       SECTORS, OR IF A CRC ERROR IS DETECTED, WRONG SECTOR   *
1228                     *       FORMAT IS DECLARED.                                    *
1229                     ****************************************************************


1231                     SSS0A   CJP    WCEMPT,SSS5
1231 P0212 3018
1232                             UJP    WAD10
1232 P0213 00A3
1233                     SSS1    SFF    SNSWDFF             ENTRY FOR SENSE VERIFY
1233 P0214 BF08
1234                     SSS2    RFF    WTOP2FF             ENTRY FOR READ/WRITE/
1234 P0215 AF06
1235                     *                                  COMPARE/CRC
1236                     SSS3    LDC    BREGD,$3C
1236 P0216 8F3C
1237                     SSS4    LDC    WCD,$FF
1237 P0217 88FF
1238                     SSS5    CJP    SECTOR,SSS0A        SEARCH FOR LEGAL SECTOR
1238 P0218 6612
1239                     *                                  PULSE WITHIN 1.6 M.S.
1240                     SSS6    CJP    SECTOR,SSS9
1240 P0219 661C
1241                             CJP    WCEMPT,SSS6
1241 P021A 3019
1242                             UJP    WAD10               MISSING INDEX/SECTOR PULSES
1242 P021B 00A3
```

```
1244                SSS9   RFFCL  AUXFF,CBITC
1244 P021C AA34
1245                SSS11  LDC    WCD,$09
1245 P021D 8809
1246                       SFF    CSFTRG
1246 P021E BF18
1247                       RFF    WTRDMP
1247 P021F AF1F
1248                       RFF    COMP1
1248 P0220 AF1A
1249                       RFFCL  COMP2,CNET
1249 P0221 AB0E
1250                       CJP    WTOP1JC,WRT1
1250 P0222 191E
1251                SSS16  CJP    WCEMPT,SSS16
1251 P0223 3023
1252                       SFF    RDGATE
1252 P0224 BF11
1253                       LDC    WCD,$2
1253 P0225 8802
1254                SSS19  CJP    WCEMPT,SSS19
1254 P0226 3026
1255                       RFF    RWMOD
1255 P0227 AF19
1256                       SFF    SELBF2
1256 P0228 BF10
1257                       RFFCL  ENBDB,RDZERO
1257 P0229 A71D
1258                       CJP    AUXJC,SSS67
1258 P022A 2458
1259                SSS24  CJP    DSKERR,SSS61
1259 P022B 5853
1260                       RFFCL  SELBF1,CWORD
1260 P022C AE17
1261                       CJP    FRSTDT,SSS24
1261 P022D 262B
1262                SSS27  CJP    WORD,SSS27
1262 P022E 2A2E
1263                       SFFCL  ENBDB,CWORD
1263 P022F BE1D
```

```
1244                  SSS9    RFFCL   AUXFF,CBITC
1244 P021C  AA34
1245                  SSS11   LDC     WCD,$09
1245 P021D  8809
1246                          RFF     WTRDMP
1246 P021E  AF1F
1247                          RFF     COMP1
1247 P021F  AF1A
1248                          RFFCL   COMP2,CNET
1248 P0220  AB0E
1249                          CJP     WTOP1JC,WRT1
1249 P0221  191E
1250                  SSS16   CJP     WCEMPT,SSS16
1250 P0222  3022
1251                          SFF     CSFTRG
1251 P0223  BF18
1252                          SFF     RDGATE
1252 P0224  BF11
1253                          LDC     WCD,$2
1253 P0225  8802
1254                  SSS19   CJP     WCEMPT,SSS19
1254 P0226  3026
1255                          RFF     RWMOD
1255 P0227  AF19
1256                          SFF     SELBF2
1256 P0228  BF10
1257                          RFFCL   ENBDB,RDZERO
1257 P0229  A71D
1258                          CJP     AUXJC,SSS67
1258 P022A  2458
1259                  SSS24   CJP     DSKERR,SSS61
1259 P022B  5853
1260                          CJP     FRSTDT,SSS24
1260 P022C  262B
1261                          RFFCL   SELBF1,CWORD
1261 P022D  AE17
1262                  SSS27   CJP     WORD,SSS27
1262 P022E  2A2E
1263                          SFFCL   ENBDB,CWORD
1263 P022F  BE1D
```

```
1286                         LDC     RAMADD,$0C
1286 P0244 840C
1287                         XOR     RAMS,BF2US,BF2UD
1287 P0245 FE60
1288                         LDC     RAMADD,$0D
1288 P0246 840D
1289                         TB      BF2US,RAMD
1289 P0247 F6A0
1290                         LDC     RAMADD,$1
1290 P0248 8401
1291                         RFF     RDGATE
1291 P0249 AF11
1292                         CJP     CRCERJC,SSS61
1292 P024A 5A53
1293                         COMPR   RAMS,BF2US
1293 P024B F368
1294                         CJP     SNSWDJC,SSS64
1294 P024C 1456
1295                         SFFCL   RWMOD,CBITC
1295 P024D BA19
1296                         CJP     ALARMJC,SSS63
1296 P024E 5455
1297                         CJP     EQUAL,SSS67
1297 P024F 1E58
1298                         DA      BREGS,BREGD
1298 P0250 CFFC
1299                         CJP     COUT,SSS61
1299 P0251 1A53
1300                         UJP     SSS4
1300 P0252 0017
1301                 SSS61   LDC     RAMADD,$7
1301 P0253 8407
1302                         LDC     RAMD,$8
1302 P0254 8608
1303                 SSS63   SFF     ALARMFF
1303 P0255 BF2F
1304                 SSS64   RFF     RDGATE
1304 P0256 AF11
1305                         UJP     WLBU1
1305 P0257 0000
```

```
                     SSS67  RFF     AUXFF
     P0258 AF34
                            RFF     CNALU
     P0259 AF20
                            LDC     RAMADD,$0
     P025A 8400
                            IA      RAMS,PCD
     P025B C708


                     ******************************************************************
                     *                                                                *
                     *                *** ADVANCE  SUBROUTINE ***                     *
                     *                                                                *
                     *      THIS SUBROUTINE COMPUTES AND DECIDES THE NEXT DISK        *
                     *     LOCATION AFTER FINISHING THE CURRENT SECTOR.               *
                     *      IF THE DATA TRANSFER EXTENDS BEYOND THE LAST SECTOR OF    *
                     *       THE "TOP" SURFACE, THE TRANSFER CONTINUES FROM THE       *
                     *     FIRST SECTOR OF THE "BOTTOM" SURFACE. IF DATA TRANSFER     *
                     *     EXTENDS BEYOND THE LAST SECTOR IN A CYLINDER, THE ADVANCE  *
                     *     SUBROUTINE TAKES CARE OF MOVING THE HEADS TO THE NEXT      *
                     *     CYLINDER AND CONTINUES THE TRANSFER FROM THERE. IF TRANSFER*
                     *     IS ATTEMPTED BEYOND THE LAST CYLINDER IN A DISK AN         *
                     *     END OF MEDIUM ERROR IS DECLARED                            *
                     *                                                                *
                     ******************************************************************

                     ADV0   LDC     WCD,$1
     P025C 8801
                     ADV1   RFF     SELBF2
     P025D AF10
                            LDC     BF2UD,$1F
     P025E 8E1F
                            LDC     RAMADD,$1
     P025F 8401
                            ANDAB   RAMS,BF2US,BREGD
     P0260 FFB0
                            LDC     BF2LD,$1C
     P0261 8D1C
```

```
1336                          MINUS   BREGS,BF2LS,NU
1336 P0262 E36C
1337                  ADV4    CJP     WCEMPT,ADV4
1337 P0263 3063
1338                          RFF     EGWG
1338 P0264 AF1C
1339                          CJP     COUT,ADV13
1339 P0265 1A6D
1340                          CJP     SNSWDJC,WLBU1
1340 P0266 1400
1341                          ANDCB   RAMS,BF2US,BREGD
1341 P0267 FF70
1342                          CJP     BMSB,ADV19
1342 P0268 5071
1343                          SFF     HS1
1343 P0269 BF0D
1344                          LDC     BF2LD,$80
1344 P026A 8D80
1345                          OR      BREGS,BF2LS,RAMD
1345 P026B E6E4
1346                          UJP     ADV15
1346 P026C 006F
1347                  ADV13   IA      RAMS,RAMD
1347 P026D C608
1348                          CJP     SNSWDJC,WAD14
1348 P026E 14A7
1349                  ADV15   LDC     RAMADD,$0
1349 P026F 8400
1350                          IA      RAMS,PCD
1350 P0270 C708
1351                  ADV19   RFF     HS1
1351 P0271 AF0D
1352                          RFF     ENWDSY
1352 P0272 AF1B
1353                          LDC     BF2UD,$0F
1353 P0273 8E0F
1354                          LDC     BF2LD,$40
1354 P0274 8D40
1355                          ANDAB   RAMS,BF2LS,RAMD
1355 P0275 E6B0
```

```
1357                           LDC     RAMADD,$2
1357 P0276 8402
1358                           PLUSI   RAMS,BF2US,RAMD
1358 P0277 F698
1359                           LDC     RAMADD,$3
1359 P0278 8403
1360                           CJP     COUT,ADV29
1360 P0279 1A7B
1361                           IA      RAMS,RAMD
1361 P027A C608
1362              ADV29        TA      RAMS,BREGD
1362 P027B CFF0
1363                           LDC     BF2LD,$B0
1363 P027C 8DB0
1364                           LDC     BF2UD,$0C
1364 P027D 8E0C
1365                           CJP     SNGDNJC,ADV35
1365 P027E 4081
1366                           LDC     BF2LD,$60
1366 P027F 8D60
1367                           LDC     BF2UD,$19
1367 P0280 8E19
1368              ADV35        MINUS   RAMS,BF2US,NU
1368 P0281 F368
1369                           LDC     RAMADD,$2
1369 P0282 8402
1370                           CJP     COUT,ADV45
1370 P0283 1A8A
1371                           MINUS   RAMS,BF2LS,NU
1371 P0284 E368
1372                           CJP     COUT,ADV45
1372 P0285 1A8A
1373                           LDC     RAMADD,$7
1373 P0286 8407
1374                           LDC     RAMD,$1
1374 P0287 8601
1375              ADV42        SFF     ALARMFF
1375 P0288 BF2F
```

```
1377                   UJP    WLBU1
1377 P0289 0000
1378           ADV45   RFF    RMBNKS
1378 P028A AF33
1379                   SFF    CNALU
1379 P028B BF20
1380                   SFF    AUXFF
1380 P028C BF34
1381                   UJP    STD14
1381 P028D 00C4
1382           ADV49   RFF    AUXFF
1382 P028E AF34
1383                   RFF    CNALU
1383 P028F AF20
1384                   SFF    ENWDSY
1384 P0290 BF1B
1385           ADV51   CJP    ONCYL,ADV15
1385 P0291 786F
1386                   CJP    SEEKER,ADV42
1386 P0292 0488
1387                   UJP    ADV51
1387 P0293 0091


1390           ****************************************************************
1391           WRT74   SFFCL  ALARMFF,CREQ     SUB SECTION OF THE WRITE ROUTINE *
1391 P0294 B52F
1392                   RFF    CSFTRG
1392 P0295 AF18
1393                   RFF    ENBDB
1393 P0296 AF1D
1394                   UJP    WRT101
1394 P0297 0183
```

```
1396                ***************************************************************
1397                *                                                             *
1398                *          *** WRITE ADDRESS COMMAND ***                      *
1399                *                                                             *
1400                *      THIS ROUTINE CAUSES THE CONTROLLER TO WRITE THE        *
1401                *      ADDRESS TAGS OF ALL THE SECTORS IN THE PRESENTLY       *
1402                *      AVAILABLE TRACK. THIS ROUTINE USES THE ADVANCE SUBROUTINE*
1403                *      TO COMPUTE THE NEXT SECTOR AND THE END OF OPERATION    *
1404                *                                                             *
1405                ***************************************************************


1407                WAD1   SFF    SNSWDFF
1407 P0298 BF08
1408                       CJP    DKWTPT,WRT79
1408 P0299 6D6D
1409                       SFF    WTRDMP
1409 P029A BF1F
1410                       LDC    BPEGD,$A0
1410 P029B 8FA0
1411                       LDC    WCD,$FF
1411 P029C 88FF
1412                WAD4   CJP    INDEX,WAD36          SEARCH FOR LEGAL INDEX
1412 P029D 56C3
1413                *                                  PULSE WITHIN 152 M.S.
1414                WAD5   LDC    WCD,$FF
1414 P029E 88FF
1415                WAD6   CJP    INDEX,WAD14
1415 P029F 56A7
1416                       CJP    WCEMPT,WAD6
1416 P02A0 309F
1417                       IA     BREGS,BREGD
1417 P02A1 CF0C
1418                       CJP    COUT,WAD5
1418 P02A2 1A9E
1419                WAD10  LDC    RAMADD,$7
1419 P02A3 8407
1420                       LDC    RAMD,$04
1420 P02A4 8604
```

```
1422                        SFF     ALARMFF
1422 P02A5 BF2F
1423                        UJP     WLBU1
1423 P02A6 0000
1424                WAD14   LDC     WCD,$FF
1424 P02A7 88FF
1425                WAD15   CJP     SECTOR,WAD16
1425 P02A8 66AB
1426                        CJP     WCEMPT,WAD15
1426 P02A9 30A8
1427                        UJP     WAD10
1427 P02AA 00A3
1428                WAD16   RFFCL   CSFTRG,CBITC
1428 P02AB AA18
1429                        SFFCL   EGWG,RDZERO
1429 P02AC B71C
1430                        LDC     BF2UD,$01
1430 P02AD 8E01
1431                        LDC     RAMADD,$03
1431 P02AE 8403
1432                        TA      RAMS,BF2LD
1432 P02AF CDF0
1433                        LDC     WCD,$0D
1433 P02B0 880D
1434                WAD22   CJP     WCEMPT,WAD22
1434 P02B1 30B1
1435                        SFFCL   CSFTRG,CWORD
1435 P02B2 BE18
1436                WAD24   CJP     WORD,WAD24
1436 P02B3 2AB3
1437                        LDC     RAMADD,$2
1437 P02B4 8402
1438                        TA      RAMS,BF2UD
1438 P02B5 CEF0
1439                        LDC     RAMADD,$1
1439 P02B6 8401
1440                        TA      RAMS,BF2LD
1440 P02B7 CDF0
1441                        LDC     RAMADD,$C
1441 P02B8 840C
```

```
1443                       XOR    RAMS,BF2LS,BF2LD
1443 P02B9 ED60
1444                       CLO    CWORD
1444 P02BA BEFF
1445              WAD30    CJP    WORD,WAD30
1445 P02BB 2ABB
1446                       SFFCL  CRCMOD,CWORD
1446 P02BC BE2B
1447              WAD30B   CJP    WORD,WAD30B
1447 P02BD 2ABD
1448                       RFFCL  CSFTRG,CWORD
1448 P02BE AE18
1449              WAD32    CJP    WORD,WAD32
1449 P02BF 2ABF
1450                       RFF    CRCMOD
1450 P02C0 AF2B
1451                       LDC    WCD,$06
1451 P02C1 8806
1452                       UJP    ADV1
1452 P02C2 005D
1453              WAD36    CJP    WCEMPT,WAD4
1453 P02C3 309D
1454                       UJP    WAD10
1454 P02C4 00A3
1455                       SPARE
1455 P02C5 FFFF
1456                       SPARE
1456 P02C6 FFFF
1457                       SPARE
1457 P02C7 FFFF
1458                       SPARE
1458 P02C8 FFFF
1459                       SPARE
1459 P02C9 FFFF
```

```
                 ****************************************************************
                 *                                                              *
                 *            *** READ AND CHECKWORD CHECK COMMANDS ***         *
                 *                                                              *
                 *       THIS ROUTINE USES THE FOLLOWING SUBROUTINES:           *
                 *       DECREMENT BLOCK LENGTH SEARCH SECTOR AND ADVANCE.      *
                 *        READ AND CHECKWORD-CHECK COMMANDS USE THE SAME        *
                 *       ROUTINE, EXCEPT FOR DIFFERENT ENTRIES.                 *
                 *        CHECKWORD-CHECK RESETS BF1ENB FLIP-FLOP SO THAT DATA  *
                 *       IS NOT TRANSFERED TO OR FROM MEMORY.                   *
                 *                                                              *
                 ****************************************************************

                 READ1  RFF     BF1ENB                ENTRY FOR CHECKWORD CHECK
P02CA AF1E
                 READ2  IA      PCS,RAMD              ENTRY FOR READ COMMAND
P02CB C60F
                        UJP     DCBL1
P02CC 0003
                        CJP     BLZROJC,WLBU1
P02CD 1000
                 READ5  IA      PCS,RAMD
P02CE C60F
                        UJP     SSS3
P02CF 0016
                        SFF     AUXFF
P02D0 BF34
                        IA      PCS,RAMD
P02D1 C60F
                        UJP     SSS11
P02D2 001D
                 READ10 CJP     DSKERR,WRT77
P02D3 5968
                        CJP     FRSTDT,READ10
P02D4 26D3
                        SFF     ENBNED
P02D5 BF0B
                        SFF     ENBDB
P02D6 BF1D
```

```
1488                          LDC    WCD,$5F
1488 P02D7 885F
1489                          LADDR  RAMD,READ20-1
1489 P02D8 86DC
1490                   READ16 SFFCL  CNALU,CWORD
1490 P02D9 BE20
1491                          LDC    RAMADD,$8
1491 P02DA 8408
1492                          DA     RAMS,RAMD
1492 P02DB C6F8
1493                          CJP    COUT,DCBL6
1493 P02DC 1A08
1494                   READ20 CJP    BLZROJC,READ59
1494 P02DD 1105
1495                   READ21 CJP    WORD,READ48
1495 P02DE 2AFA
1496                          CJP    BF1F,READ25
1496 P02DF 32E2
1497                          RFFCL  PRIOR,CWORD
1497 P02E0 AE07
1498                          UJP    READ26
1498 P02E1 00E3
1499                   READ25 SFFCL  PRIOR,CWORD
1499 P02E2 BE07
1500                   READ26 CJP    WCEMPT,READ16
1500 P02E3 30D9
1501                   READ27 CJP    DSKERR,WRT77
1501 P02E4 596B
1502                          CJP    WORD,READ27
1502 P02E5 2AE4
1503                   READ29 CJP    HFWRD,READ31
1503 P02E6 3AE8
1504                          UJP    READ29
1504 P02E7 00E6
1505                   READ31 RFFCL  CNALU,CRCERCL
1505 P02E8 A420
1506                          RFF    ENBNED
1506 P02E9 AF0B
1507                          IA     PCS,RAMD
1507 P02EA C60F
```

```
1509                     UJP    DCBL1
1509 P02EB 0003
1510                     RFF    RDGATE
1510 P02EC AF11
1511                     CJP    BF1F,READ80
1511 P02ED 331A
1512                     RFF    ENBDB
1512 P02EE AF1D
1513                     SFF    RWMOD
1513 P02EF BF19
1514                     LDC    RAMADD,$0B
1514 P02F0 840B
1515                     TB     BF2US,RAMD
1515 P02F1 F6A0
1516                     LDC    RAMADD,$0A
1516 P02F2 840A
1517                     TB     BF2LS,RAMD
1517 P02F3 E6A0
1518                     CJP    CRCERJC,READ78
1518 P02F4 5B18
1519                     CJP    ALARMJC,READ81
1519 P02F5 551B
1520                     CJP    BLZROJC,READ81
1520 P02F6 111B
1521                     IA     PCS,RAMD
1521 P02F7 C60F
1522                     UJP    ADV0
1522 P02F8 005C
1523                     UJP    READ5
1523 P02F9 00CE
1524              READ48 CJP    DSKERR,WRT77          ERRORS LOOP
1524 P02FA 596B
1525                     CJP    PRTFLT,READ54
1525 P02FB 1700
1526                     CJP    ADRERR,READ56
1526 P02FC 0702
1527                     CJP    PARERR,READ56
1527 P02FD 0B02
1528                     CJP    LSTDT,READ56
1528 P02FE 3F02
```

```
1530                         UJP     READ21
1530 P02FF 00DE
1531                 READ54  LDC     RAMADD,$6
1531 P0300 8406
1532                         LDC     RAMD,$02
1532 P0301 8602
1533                 READ56  SFF     ALARMFF
1533 P0302 BF2F
1534                         RFFCL   ENBNED,CREQ
1534 P0303 A50B
1535                         UJP     READ68
1535 P0304 010E
1536                 READ59  CJP     DSKERR,WRT77
1536 P0305 596B
1537                         CJP     WORD,READ59
1537 P0306 2B05
1538                         RFFCL   AUXFF,CWORD
1538 P0307 AE34
1539                         CJP     WCEMPT,READ64
1539 P0308 310A
1540                         SFF     AUXFF
1540 P0309 BF34
1541                 READ64  CJP     DSKERR,WRT77
1541 P030A 596B
1542                         CJP     BF2F,READ74
1542 P030B 0F14
1543                         RFF     ENBNED
1543 P030C AF0B
1544                         CJP     BF2F,READ64
1544 P030D 0F0A
1545                 READ68  RFF     ENBDB
1545 P030E AF1D
1546                         CJP     AUXJC,READ27
1546 P030F 24E4
1547                 READ70  CJP     DSKERR,WRT77
1547 P0310 596B
1548                         CJP     WCEMPT,READ70
1548 P0311 3110
1549                         CLO     CWORD
1549 P0312 BEFF
```

```
1551                   UJP     READ27
1551 P0313 00E4
1552            READ74 CJP     WORD,READ64
1552 P0314 2B0A
1553                   LDC     RAMADD,$6
1553 P0315 8406
1554                   LDC     RAMD,$08
1554 P0316 8608
1555                   UJP     READ56
1555 P0317 0102
1556            READ78 LDC     RAMADD,$6
1556 P0318 8406
1557                   LDC     RAMD,$10
1557 P0319 8610
1558            READ80 SFF     ALARMFF
1558 P031A BF2F
1559            READ81 RFF     RMBNKS
1559 P031B AF33
1560                   RFF     SELBF2
1560 P031C AF10
1561                   UJP     WL1
1561 P031D 0040
```



```
1563            ***********************************************************
1564            *                                                         *
1565            *        *** WRITE DATA AND COMPARE COMMANDS ***          *
1566            *                                                         *
1567            *       THIS ROUTINE USES THE FOLLOWING SUBROUTINES :     *
1568            *       DECREMENT BLOCK LENGTH,SEARCH SECTOR,ADVANCE,     *
1569            *       TWO LAST WORDS AND DECREMENT THREE WORDS.         *
1570            *                                                         *
1571            *        WRITE AND COMPARE COMMANDS USE THE SAME ROUTINE, *
1572            *       EXCEPT FOR DIFFERENT ENTRIES TO THE PROGRAM.      *
1573            *        COMPARE SETS COMPARE INDEX FLIP-FLOP AND THEREFORE *
1574            *       SPECIAL INSTRUCTIONS ARE EXCECUTED, WHEN NEEDED, FOR *
1575            *       THE COMPARE FUNCTION.                             *
1576            *                                                         *
1577            ***********************************************************

1579            *                          DECREMENT THREE WORDS SUBROUTINE:  *
1580            WRT1   CJP     WTOP2JC,SSS16        AT THE BEGINNING OF EVERY
1580 P031E 4C23
1581                   RFF     BL1FF                SECTOR THE BLOCK LENGTH
1581 P031F AF32
1582                   IA      PCS,RAMD             REGISTER IS DECREMENTED
1582 P0320 C60F
1583                   UJP     DCBL1                BY THREE SO THAT THE MICRO
1583 P0321 0003
1584                   CJP     BLZROJC,WRT63        CAN STOP IN TIME THE
1584 P0322 115D
1585                   IA      PCS,RAMD             AUTOMATIC DOUBLE BUFFER
1585 P0323 C60F
1586                   UJP     DCBL1
1586 P0324 0003
1587                   CJP     BLZROJC,WRT12
1587 P0325 1129
1588                   IA      PCS,RAMD
1588 P0326 C60F
1589                   UJP     DCBL1
1589 P0327 0003
1590                   CJP     BLZROJC,WRT62
1590 P0328 115C
```

```
1592                 WRT12  SFF    WTOP2FF
1592 P0329 BF06
1593                        LADDR  RAMD,WRT22-1
1593 P032A 8633
1594                        UJP    SSS16
1594 P032B 0023
1595                 WRT14  SFF    COMPFF             ENTRY FOR COMPARE COMAND.
1595 P032C BF30
1596                        UJP    WRT17
1596 P032D 012F
1597                 WRT16  CJP    DKWTPT,WRT79       ENTRY FOR WRITE DATA COMMAND
1597 P032E 6D6D
1598                 WRT17  SFF    WTOP1FF
1598 P032F BF09
1599                        IA     PCS,RAMD
1599 P0330 C60F
1600                        UJP    DCBL1
1600 P0331 0003
1601                        CJP    BLZROJC,WLBU1
1601 P0332 1000
1602                 WRT21  UJP    SSS2
1602 P0333 0015
1603                 WRT22  SFF    SELBF1
1603 P0334 BF17
1604                        SFF    WTRDMP
1604 P0335 BF1F
1605                        CJP    COMPJC,WRT83
1605 P0336 2171
1606                        RFF    CSFTRG
1606 P0337 AF18
1607                        LDC    WCD,$5
1607 P0338 8805
1608                 WRT27  CJP    WCEMPT,WRT27
1608 P0339 3139
1609                        SFFCL  EGWG,RDZERO
1609 P033A B71C
1610                        LDC    WCD,$7
1610 P033B 8807
1611                 WRT30  CJP    WCEMPT,WRT30
1611 P033C 313C
```

```
1613                            SFFCL   ENBDB,SBF2F
1613 P033D B91D
1614                  WRT32     CJP     BLZROJC,WRT99
1614 P033E 1181
1615                  WRT33     SFF     ENBNED
1615 P033F BF0B
1616                  WRT34     SFFCL   ENBDB,DMAREQ
1616 P0340 B21D
1617                            CJP     COMPJC,WRT90
1617 P0341 2178
1618                            RFFCL   SELBF2,CWORD
1618 P0342 AE10
1619                            LDC     BF2LD,$01
1619 P0343 8D01
1620                            LDC     BF2UD,$00
1620 P0344 8E00
1621                            SFF     SELBF2
1621 P0345 BF10
1622                            SFF     CSFTRG
1622 P0346 BF18
1623                  WRT41     CJP     WORD,WRT41
1623 P0347 2B47
1624                            CJP     BLZROJC,WRT65
1624 P0348 115F
1625                            CLO     CWORD
1625 P0349 BEFF
1626                  WRT44     CJP     WORD,WRT44
1626 P034A 2B4A
1627                  WRT45     LDC     WCD,$5D
1627 P034B 885D
1628                            CJP     BLZROJC,WRT141
1628 P034C 11AB
1629                            CJP     BL1JC,WRT144
1629 P034D 39AE
1630                            LADDR   RAMD,WRT53-1
1630 P034E 8652
1631                  WRT49     SFFCL   CNALU,CWORD
1631 P034F BE20
1632                            LDC     RAMADD,$8
1632 P0350 8408
```

```
1634                       DA     RAMS,RAMD
1634 P0351 C6F8
1635                       CJP    COUT,DCBL6
1635 P0352 1A08
1636             WRT53     CJP    BLZROJC,WRT146
1636 P0353 11B0
1637             WRT54     CJP    WORD,WRT69
1637 P0354 2B63
1638                       RFFCL  PRIOR,CWORD
1638 P0355 AE07
1639                       CJP    BF2F,WRT58
1639 P0356 0F58
1640                       SFF    PRIOR
1640 P0357 BF07
1641             WRT58     CJP    WCEMPT,WRT49        END OF SECTOR
1641 P0358 314F
1642                       LDC    RAMADD,$0
1642 P0359 8400
1643                       LADDR  RAMD,WRT107-1
1643 P035A 8688
1644                       UJP    WRT146
1644 P035B 01B0
1645             WRT62     RFF    BLZROFF
1645 P035C AF0A
1646             WRT63     SFF    BL1FF
1646 P035D BF32
1647                       UJP    WRT12
1647 P035E 0129
1648             WRT65     CJP    HFWRD,WRT67
1648 P035F 3B61
1649                       UJP    WRT65
1649 P0360 015F
1650             WRT67     RFFCL  ENBNED,CWORD
1650 P0361 AE0B
1651                       UJP    WRT44
1651 P0362 014A
1652             WRT69     CJP    LSTDT,WRT74         ERRORS LOOP
1652 P0363 3E94
1653                       CJP    ADRERR,WRT74
1653 P0364 0694
```

```
1655                        CJP     PARERR,WRT74
1655 P0365 0A94
1656                        CJP     DSKERR,WRT77
1656 P0366 596B
1657                        UJP     WRT54
1657 P0367 0154
1658                        SPARE
1658 P0368 FFFF
1659                        SPARE
1659 P0369 FFFF
1660                        SPARE
1660 P036A FFFF
1661            WRT77       LDC     RAMADD,$7
1661 P036B 8407
1662                        LDC     RAMD,$10
1662 P036C 8610
1663            WRT79       SFFCL   ALARMFF,CREQ
1663 P036D B52F
1664                        RFF     RDGATE
1664 P036E AF11
1665            WRT81       RFF     EGWG
1665 P036F AF1C
1666                        UJP     READ81
1666 P0370 011B
1667            WRT83       SFF     COMP1
1667 P0371 BF1A
1668                        SFF     AUXFF
1668 P0372 BF34
1669                        LDC     WCD,$8
1669 P0373 8808
1670                        IA      PCS,RAMD
1670 P0374 C60F
1671                        UJP     SSS16
1671 P0375 0023
1672                        RFFCL   ENWDSY,CNET
1672 P0376 AB1B
1673                        UJP     WRT32
1673 P0377 013E
1674            WRT90       CJP     DSKERR,WRT77
1674 P0378 596B
```

```
1676                          CJP     FRSTDT,WRT90
1676 P0379 2778
1677                          CJP     BLZROJC,WRT94
1677 P037A 117C
1678                          UJP     WRT95
1678 P037B 017D
1679              WRT94       RFF     ENBNED
1679 P037C AF0B
1680              WRT95       RFF     ENBDB
1680 P037D AF1D
1681                          SFFCL   ENBDB,CWORD
1681 P037E BE1D
1682                          SFFCL   ENWDSY,SBF1F
1682 P037F B81B
1683                          UJP     WRT45
1683 P0380 014B
1684              WRT99       CJP     BL1JC,WRT34
1684 P0381 3940
1685                          UJP     WRT33
1685 P0382 013F
1686              WRT101      CJP     DSKERR,WRT77
1686 P0383 596B
1687                          CJP     WCEMPT,WRT101
1687 P0384 3183
1688                          CLO     CWORD
1688 P0385 BEFF
1689              WRT104      CJP     WORD,WRT104
1689 P0386 2B86
1690                          CLO     CWORD
1690 P0387 BEFF
1691              WRT106      CJP     WORD,WRT106
1691 P0388 2B88
1692              WRT107      CJP     COMPJC,WRT123
1692 P0389 2199
1693                          SFFCL   CRCMOD,CWORD
1693 P038A BE2B
1694              WRT109      CJP     WORD,WRT109
1694 P038B 2B8B
1695                          RFFCL   CSFTRG,CWORD
1695 P038C AE18
```

```
1697                   WRT111 CJP     WORD,WRT111
1697 P038D 2B8D
1698                   WRT112 RFFCL   CRCMOD,CBITC
1698 P038E AA2B
1699                          LDC     WCD,$3
1699 P038F 8803
1700                          SFF     RWMOD
1700 P0390 BF19
1701                          RFF     RDGATE
1701 P0391 AF11
1702                          CJP     ALARMJC,WRT121
1702 P0392 5597
1703                          CJP     BLZROJC,WRT121
1703 P0393 1197
1704                          IA      PCS,RAMD
1704 P0394 C60F
1705                          UJP     ADV1
1705 P0395 005D
1706                          UJP     WRT21
1706 P0396 0133
1707                   WRT121 CJP     WCEMPT,WRT121
1707 P0397 3197
1708                          UJP     WRT81
1708 P0398 016F
1709                   WRT123 CLO     CWORD
1709 P0399 BEFF
1710                   WRT124 CJP     WORD,WRT124
1710 P039A 2B9A
1711                   WRT125 CJP     HFWRD,WRT127
1711 P039B 3B9D
1712                          UJP     WRT125
1712 P039C 019B
1713                   WRT127 SFFCL   JGRP9,CRCERCL
1713 P039D B429
1714                          NOOP
1714 P039E BFFF
1715                          LDC     RAMADD,$6
1715 P039F 8406
1716                          CJP     NOCOMP,WRT136
1716 P03A0 05A6
```

```
1718                             RFF      JGRP9
1718 P03A1 AF29
1719                             CJP      CRCERJC,WRT134
1719 P03A2 5BA4
1720                             UJP      WRT112
1720 P03A3 018E
1721                     WRT134  LDC      RAMD,$10
1721 P03A4 8610
1722                             UJP      WRT79
1722 P03A5 016D
1723                     WRT136  RFF      JGRP9
1723 P03A6 AF29
1724                             LDC      RAMD,$30
1724 P03A7 8630
1725                             CJP      CRCERJC,WRT79
1725 P03A8 5B6D
1726                             LDC      RAMD,$20
1726 P03A9 8620
1727                             UJP      WRT79
1727 P03AA 016D
1728                     WRT141  LADDR    RAMD,WRT101-1
1728 P03AB 8682
1729                             CJP      BL1JC,WRT156
1729 P03AC 39BA
1730                             UJP      WRT151
1730 P03AD 01B5
1731                     WRT144  SFF      BLZROFF              TWO LAST WORDS SUBROUTINE
1731 P03AE BF0A
1732                             CJP      COMPJC,WRT164
1732 P03AF 21C2
1733                     WRT146  CJP      BF2F,WRT148
1733 P03B0 0FB2
1734                             CJP      WORD,WRT146
1734 P03B1 2BB0
1735                     WRT148  RFF      ENBNED
1735 P03B2 AF0B
1736                     WRT149  CJP      WORD,WRT149
1736 P03B3 2BB3
1737                             CJP      BLZROJC,WRT164
1737 P03B4 11C2
```

```
1739                   WRT151 RFFCL   CNALU,CWORD
1739 P03B5 AE20
1740                   WRT152 CJP     WORD,WRT152
1740 P03B6 2BB6
1741                          CJP     LSTDT,WRT155
1741 P03B7 3FB9
1742                          UJP     WRT156
1742 P03B8 01BA
1743                   WRT155 SFF     ALARMFF
1743 P03B9 BF2F
1744                   WRT156 RFFCL   ENBDB,CWORD
1744 P03BA AE1D
1745                          CJP     COMPJC,WRT162
1745 P03BB 21C0
1746                          RFF     SELBF2
1746 P03BC AF10
1747                          LDC     BF2UD,$00
1747 P03BD 8E00
1748                          LDC     BF2LD,$00
1748 P03BE 8D00
1749                          IA      RAMS,PCD
1749 P03BF C708
1750                   WRT162 SFF     COMP2
1750 P03C0 BF0E
1751                          IA      RAMS,PCD
1751 P03C1 C708
1752                   WRT164 RFFCL   ENBNED,CWORD
1752 P03C2 AE0B
1753                          LADDR   RAMD,WRT101-1
1753 P03C3 8682
1754                          CJP     WCEMPT,WRT168
1754 P03C4 31C6
1755                          LADDR   RAMD,WRT107-1
1755 P03C5 8688
1756                   WRT168 CJP     WORD,WRT168
1756 P03C6 2BC6
1757                          CJP     WCEMPT,WRT151
1757 P03C7 31B5
1758                          LADDR   RAMD,WRT106-1
1758 P03C8 8687
```

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                        UJP     WRT151
      P03C9 01B5
                        SPARE
      P03CA FFFF
                        SPARE
      P03CB FFFF

                   ****************************************************************
                   *                                                              *
                   *               *** SELF TEST 2 UPPER SECTION ***              *
                   *                                                              *
                   ****************************************************************

                   T2U74  CJP     WTOP2JC,T2U91
      P03CC 4DDD
                          CJP     SNGDNJC,T2U91
      P03CD 41DD
                          CJP     BL1JC,T2U91
      P03CE 39DD
                          LDC     RAMADD,$4
      P03CF 8404
                          CJP     AUXJC,T2U91
      P03D0 25DD
                          CJP     COMPJC,T2U91
      P03D1 21DD
                          CJP     BF2F,T2U91
      P03D2 0FDD
                          CJP     LSTDT,T2U91
      P03D3 3FDD
                          SFF     BLZROFF
      P03D4 BF0A
                          SFF     ALARMFF
      P03D5 BF2F
                          SFF     WTOP2FF
      P03D6 BF06
                          SFF     SNGDNFF
      P03D7 BF02
                          SFF     BL1FF
      P03D8 BF32
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1784                        LDC      RAMD,$10
1784 P03D9 8610
1785                        SFF      AUXFF
1785 P03DA BF34
1786                        SFFCL    COMPFF,FRINXCL
1786 P03DB B630
1787                        CJP      ONBUSJC,T2U93
1787 P03DC 3DDF
1788               T2U91    RFF      RMBNKS
1788 P03DD AF33
1789                        UJP      TST258
1789 P03DE 01F0
1790               T2U93    CJP      ALDENJC,T2U95
1790 P03DF 1DE1
1791                        UJP      T2U91
1791 P03E0 01DD
1792               T2U95    CJP      WTOP1JC,T2U97
1792 P03E1 19E3
1793                        UJP      T2U91
1793 P03E2 01DD
1794               T2U97    CJP      SNSWDJC,T2U99
1794 P03E3 15E5
1795                        UJP      T2U91
1795 P03E4 01DD
1796               T2U99    CJP      BLZROJC,T2U101
1796 P03E5 11E7
1797                        UJP      T2U91
1797 P03E6 01DD
1798               T2U101   CJP      ALARMJC,T2U103
1798 P03E7 55E9
1799                        UJP      T2U91
1799 P03E8 01DD
1800               T2U103   CJP      WTOP2JC,T2U105
1800 P03E9 4DEB
1801                        UJP      T2U91
1801 P03EA 01DD
1802               T2U105   CJP      SNGDNJC,T2U107
1802 P03EB 41ED
1803                        UJP      T2U91
1803 P03EC 01DD
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1805                 T2U107 CJP    BL1JC,T2U109
1805 P03ED 39EF
1806                        UJP    T2U91
1806 P03EE 01DD
1807                 T2U109 CJP    AUXJC,T2U111
1807 P03EF 25F1
1808                        UJP    T2U91
1808 P03F0 01DD
1809                 T2U111 CJP    COMPJC,T2U113
1809 P03F1 21F3
1810                        UJP    T2U91
1810 P03F2 01DD
1811                 T2U113 CJP    FRINXJC,T2U115
1811 P03F3 53F5
1812                        UJP    T2U91
1812 P03F4 01DD
1813                 T2U115 CJP    LSTDT,T2U117
1813 P03F5 3FF7
1814                        UJP    T2U91
1814 P03F6 01DD
1815                 T2U117 LDC    AOUTLD,$ED
1815 P03F7 8CED
1816                        LDC    AOUTUD,$AC
1816 P03F8 89AC
1817                        UJP    WLBU1
1817 P03F9 0000
1818                        SPARE
1818 P03FA FFFF
1819                        SPARE
1819 P03FB FFFF
1820                        SPARE
1820 P03FC FFFF
1821                        SPARE
1821 P03FD FFFF
1822                        SPARE
1822 P03FE FFFF
1823                        SPARE
1823 P03FF FFFF
1824                       END     START1

PGM=  0400 (  1024)   COM = 0000 (      0)   DAT = 0000 (      0)
```

E Q U I V A L E N C E S

DEF.LINE	NAME	VALUE		REFERENCED AT LINE NUMBER
0000	I	00FF	(000255)	
0251	MODE0	0000	(000000)	
0252	MODE1	0001	(000001)	
0253	MODE2	0002	(000002)	
0254	MODE3	0003	(000003)	
0255	MODE4	0004	(000004)	
0256	MODE5	0005	(000005)	
0258	MODE6	0006	(000006)	
0259	MODE7	0007	(000007)	
0260	MODE8	0008	(000008)	
0261	MODE9	0009	(000009)	
0262	MODEA	000A	(000010)	
0264	MODEB	000B	(000011)	
0265	MODEC	000C	(000012)	
0266	MODED	000D	(000013)	
0267	MODEE	000E	(000014)	
0268	MODEF	000F	(000015)	0527
0272	NU	0003	(000003)	0527, 0640, 1142, 1336, 1368, 1371
0273	RAMADD	0004	(000004)	0455, 0545, 0588, 0614, 0620, 0639, 0659, 0661, 0671, 0673, 0693, 0695, 0705, 0774, 0778, 0831 0839, 0853, 0855, 0935, 1019, 1029, 1061, 1068, 1086, 1089, 1091, 1093, 1095, 1202, 1206, 1210 1266, 1268, 1270, 1274, 1280, 1286, 1288, 1290, 1301, 1309, 1332, 1349, 1357, 1359, 1369, 1373 1419, 1431, 1437, 1439, 1441, 1491, 1514, 1516, 1531, 1553, 1556, 1632, 1642, 1661, 1715, 1773
0274	BANKD	0005	(000005)	0465, 1085
0275	RAMD	0006	(000006)	0456, 0546, 0592, 0596, 0600, 0621, 0660, 0662, 0694, 0696, 0709, 0712, 0775, 0779, 0832, 0854 0856, 0937, 0973, 0976, 1025, 1062, 1064, 1071, 1073, 1078, 1080, 1087, 1090, 1092, 1094, 1096 1203, 1207, 1267, 1269, 1281, 1289, 1302, 1345, 1347, 1355, 1358, 1361, 1374, 1420, 1475, 1478 1481, 1489, 1492, 1507, 1515, 1517, 1521, 1532, 1554, 1557, 1582, 1585, 1588, 1593, 1599, 1630 1634, 1643, 1662, 1670, 1704, 1721, 1724, 1726, 1728, 1753, 1755, 1758, 1784
0276	PCD	0007	(000007)	0651, 0865, 1030, 1211, 1310, 1350, 1749, 1751
0277	WCD	0008	(000008)	0612, 0788, 0791, 0795, 0802, 0864, 1022, 1130, 1237, 1245, 1253, 1329, 1411, 1414, 1424, 1433 1451, 1488, 1607, 1610, 1627, 1669, 1699
0278	AOUTUD	0009	(000009)	0507, 0510, 0512, 0515, 0674, 0684, 0977, 1168, 1816
0279	CWALD	000A	(000010)	0759, 0899, 1021, 1084, 1121
0281	CWAUD	000B	(000011)	0760, 0962, 1020, 1083
0283	AOUTLD	000C	(000012)	0672, 0683, 0888, 0972, 1009, 1167, 1815
0284	BF2LD	000D	(000013)	0529, 0591, 0595, 0599, 0646, 0708, 0786, 0789, 0792, 0796, 0822, 0881, 0885, 0936, 0960, 0986 1024, 1334, 1344, 1354, 1363, 1366, 1432, 1440, 1443, 1619, 1748
0285	BF2UD	000E	(000014)	0613, 0784, 0838, 0961, 0987, 1026, 1283, 1287, 1331, 1353, 1364, 1367, 1430, 1438, 1620, 1747

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0286  BREGD   000F  (000015)  0466, 0615, 0706, 0714, 0723, 0777, 0782, 0783, 0785, 0793, 0801, 0826, 0841, 0842, 0875, 0877
                              0879, 0882, 0886, 0915, 0939, 0945, 0959, 0965, 0966, 0967, 0969, 0970, 0971, 1018, 1027, 1070
                              1074, 1077, 1120, 1136, 1236, 1298, 1333, 1341, 1362, 1410, 1417
0290  RAMS    0000  (000000)  0592, 0596, 0600, 0615, 0640, 0672, 0674, 0709, 0714, 0777, 0785, 0838, 0841, 1026, 1030, 1203
                              1207, 1211, 1271, 1275, 1287, 1293, 1310, 1333, 1341, 1347, 1350, 1355, 1358, 1361, 1362, 1368
                              1371, 1432, 1438, 1440, 1443, 1492, 1634, 1749, 1751
0291  WCS     0001  (000001)  0651, 0789, 0792, 0796, 0865, 1024
0292  AINLS   0002  (000002)  0466, 0660, 0694, 0706, 0723, 0759, 0779, 0822, 0823, 0899, 0915, 0961, 0962, 0986
0293  AINUS   0003  (000003)  0465, 0662, 0696, 0760, 0775, 0832, 0959, 0960, 0987
0294  BREGS   0004  (000004)  0671, 0673, 0708, 0712, 0782, 0783, 0784, 0793, 0802, 0842, 0879, 0882, 0886, 0888, 0904, 0937
                              0939, 0945, 0965, 0966, 0967, 0969, 0970, 0971, 0972, 1019, 1027, 1122, 1136, 1142, 1146, 1298
                              1336, 1345, 1417
0295  QS      0005  (000005)  0646, 0647
0296  PCS     0007  (000007)  0527, 0973, 1475, 1478, 1481, 1507, 1521, 1582, 1585, 1588, 1599, 1670, 1704
0300  CWALS   0000  (000000)  0683, 0904, 1022, 1122, 1136
0302  CWAUS   0001  (000001)  0684, 0967, 1021
0304  BF2LS   0002  (000002)  0592, 0596, 0600, 0647, 0651, 0709, 0789, 0792, 0796, 0801, 0823, 0826, 0865, 0882, 0886, 0937
                              0970, 0972, 1009, 1025, 1269, 1275, 1336, 1345, 1355, 1371, 1443, 1517
0305  BF2US   0003  (000003)  0527, 0673, 0802, 0841, 0879, 0971, 0976, 0977, 1020, 1142, 1146, 1267, 1271, 1287, 1289, 1293
                              1333, 1341, 1358, 1368, 1515
0309  REJ     0001  (000001)  0649
0310  DMAREQ  0002  (000002)  1005, 1616
0311  RPLY    0003  (000003)  0726, 0729, 0781, 0834, 0889, 0901, 0928, 0964, 1004, 1109
0312  CRCERC  0004  (000004)  0629, 1111, 1278, 1505, 1713
0314  CREQ    0005  (000005)  1391, 1534, 1663
0315  FRINXC  0006  (000006)  0544, 1786
0316  RDZERO  0007  (000007)  1145, 1257, 1429, 1609
0318  SBF1F   0008  (000008)  1157, 1158, 1265, 1682
0319  SBF2F   0009  (000009)  1613
0320  CBITC   000A  (000010)  0852, 1118, 1244, 1295, 1428, 1698
0321  CNET    000B  (000011)  0850, 1003, 1156, 1162, 1249, 1672
0322  CDMAER  000D  (000013)  0851, 1116
0323  CWORD   000E  (000014)  1177, 1260, 1263, 1435, 1444, 1446, 1448, 1490, 1497, 1499, 1538, 1549, 1618, 1625, 1631, 1638
                              1650, 1681, 1688, 1690, 1693, 1695, 1709, 1739, 1744, 1752
0333  ADRERR  0003  (000003)  0589, 1174, 1526, 1653
0334  ALARMJ  002A  (000042)  0618, 1181, 1296, 1519, 1702, 1798
0335  ALDFXD  003E  (000062)  1063
0336  ALDENJ  000E  (000014)  0530, 1065, 1112, 1790
0337  AUTOLD  0027  (000039)  0634, 1039
0338  ALTFRC  002E  (000046)  0454
0339  AUXJC   0012  (000018)  0740, 0808, 0887, 1258, 1546, 1774, 1807
0340  BF1F    0019  (000025)  1159, 1170, 1496, 1511
0341  BF2F    0007  (000007)  1006, 1165, 1542, 1544, 1639, 1733, 1776
0342  BLZROJ  0008  (000008)  1180, 1477, 1494, 1520, 1584, 1587, 1590, 1601, 1614, 1624, 1628, 1636, 1677, 1703, 1737, 1796
0343  BL1JC   001C  (000028)  1629, 1684, 1729, 1772, 1805
0344  BMDL    0014  (000020)  0623, 0731, 0790, 0799, 0827, 0938, 0940, 0946, 1132, 1140
0345  BMSB    0028  (000040)  0617, 0707, 0724, 0787, 0794, 0836, 0847, 0916, 0926, 1134, 1141, 1342
0346  BUSBSY  002F  (000047)  0632, 0732, 0737, 0750
0347  COMPJC  0010  (000016)  1605, 1617, 1692, 1732, 1745, 1775, 1809
0348  COUT    000D  (000013)  0643, 0844, 1028, 1126, 1137, 1143, 1150, 1204, 1208, 1299, 1339, 1360, 1370, 1372, 1418, 1493
                              1635
0349  CRCERJ  002D  (000045)  1161, 1292, 1518, 1719, 1725
0350  CWAUL   001B  (000027)  0508
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0352     CWAUM    0017     (000023)     0509, 0514
0354     DKWTPT   0036     (000054)     1408, 1597
0355     DSKERR   002C     (000044)     1259, 1276, 1483, 1501, 1524, 1536, 1541, 1547, 1656, 1674, 1686
0356     EQUAL    000F     (000015)     0648, 0824, 0905, 1124, 1149, 1272, 1279, 1297
0357     FRINXJ   0029     (000041)     0616, 0626, 1115, 1811
0358     FRSTDT   0013     (000019)     1147, 1155, 1261, 1484, 1676
0359     HFWRD    001D     (000029)     1123, 1138, 1503, 1648, 1711
0360     INDEX    002B     (000043)     1412, 1415
0361     LSTDT    001F     (000031)     0597, 1007, 1528, 1652, 1741, 1777, 1813
0362     MSW1     0004     (000004)     1069
0363     MSW2     000A     (000010)     1072, 1079
0364     NOCOMP   0002     (000002)     1163, 1716
0366     ONBUSJ   001E     (000030)     0631, 0769, 0818, 0898, 0914, 1040, 1787
0367     ONCYL    003C     (000060)     0532, 0772, 0859, 1385
0368     ONOFLN   0023     (000035)     0531, 0636, 1192
0369     PARERR   0005     (000005)     0593, 1172, 1527, 1655
0370     PRTFLT   000B     (000011)     1171, 1525
0371     PRGPRT   0006     (000006)     0829, 0920, 0988
0372     RMEXEC   0004     (000004)     0627, 0630, 0633, 0638, 0641
0373     SEEKER   0002     (000002)     0533, 0858, 1386
0374     SECTOR   0033     (000051)     1238, 1240, 1425
0375     SNGDNJ   0020     (000032)     1365, 1771, 1802
0376     SKCMP0   003D     (000061)     0878
0377     SKCMP1   003B     (000059)     0876
0378     SKCMP2   0037     (000055)     0880
0379     SKCMP3   0035     (000053)     0883
0380     SNSWDJ   000A     (000010)     1114, 1294, 1340, 1348, 1794
0381     UNRDY    003A     (000058)     0770, 0819, 1050, 1053, 1056, 1059
0382     UNTPRT   0024     (000036)     0917
0383     USNGDN   0006     (000006)     0932
0384     WCEMPT   0018     (000024)     1151, 1175, 1231, 1241, 1251, 1254, 1337, 1416, 1426, 1434, 1453, 1500, 1539, 1548, 1608, 1611
                                        1641, 1687, 1707, 1754, 1757
| 0385   WORD     0015     (000021)     1128, 1154, 1178, 1262, 1277, 1436, 1445, 1447, 1449, 1495, 1502, 1537, 1552, 1623, 1626, 1637
                                        1689, 1691, 1694, 1697, 1710, 1734, 1736, 1740, 1756
0386     WTOP1J   000C     (000012)     1113, 1250, 1792
0387     WTOP2J   0026     (000038)     1580, 1770, 1800
0391     ALARMF   002F     (000047)     0526, 0544, 0849, 0860, 1282, 1303, 1375, 1391, 1422, 1533, 1558, 1663, 1743, 1779
0392     ALDENF   000C     (000012)     0604, 1043, 1157
0393     AUXFF    0034     (000052)     0605, 0730, 0902, 1244, 1307, 1380, 1382, 1480, 1538, 1540, 1668, 1785
0394     BF1ENB   001E     (000030)     0610, 1474
0395     BLZROF   000A     (000010)     0850, 1212, 1645, 1731, 1778
0396     BL1FF    0032     (000050)     1581, 1646, 1782
0397     BUSY     002E     (000046)     0628, 0729, 0780, 0833, 0900, 0927, 0963, 1003, 1108
0398     CABIT0   0031     (000049)     0798, 0800
0399     CASTRB   0036     (000054)     0803, 0806
0400     CNALU    0020     (000032)     0611, 0857, 0968, 1201, 1209, 1265, 1308, 1379, 1383, 1490, 1505, 1631, 1739
0401     CNTPRT   0000     (000000)     0918, 0921
0402     COMPFF   0030     (000048)     0603, 1595, 1786
0404     COMP1    001A     (000026)     0999, 1248, 1667
0405     COMP2    000E     (000014)     1249, 1750
0406     CRCMOD   002B     (000043)     1446, 1450, 1693, 1698
0407     CSFTRG   0018     (000024)     1116, 1246, 1392, 1428, 1435, 1448, 1606, 1622, 1695
0408     DMWRPT   002C     (000044)     0828, 0830, 0989, 1042
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0409    EGWG    001C   (000028)   1338, 1429, 1609, 1665
0410    ENBDB   001D   (000029)   0607, 1005, 1156, 1257, 1263, 1278, 1393, 1486, 1512, 1545, 1613, 1616, 1680, 1681, 1744
0411    ENBNED  000B   (000011)   1485, 1506, 1534, 1543, 1615, 1650, 1679, 1735, 1752
0412    ENWDSY  001B   (000027)   0606, 0852, 1117, 1352, 1384, 1672  `682
0413    EOP     0003   (000003)   0629, 0728, 0781, 0834, 0889, 0901   928, 0964, 1004, 1109
0414    FRCBUS  002A   (000042)   0742, 0748
0415    HS1     000D   (000013)   0843, 0845, 1343, 1351
0416    HS2     0013   (000019)   0846, 0848
0417    INTRSP  0028   (000040)   0625, 0644, 0713
0418    JGRP9   0029   (000041)   0929, 0934, 1066, 1075, 1081, 1162, 1164, 1166, 1713, 1718, 1723
0419    ONBUSF  0023   (000035)   0726, 0739, 1107
0420    PRIOR   0007   (000007)   1497, 1499, 1638, 1640
0421    RDGATE  0011   (000017)   1252, 1291, 1304, 1510, 1664, 1701
0422    RMBNKS  0033   (000051)   0807, 0863, 1182, 1191, 1378, 1559, 1788
0423    RQBUS1  0022   (000034)   0725, 0734, 0743, 0745, 0749
0424    RQBUS2  000F   (000015)   0735, 0738, 0747
0425    RTZS    0014   (000020)   0524, 0528
0426    RWMOD   0019   (000025)   0851, 1118, 1255, 1295, 1513, 1700
0427    SELBF1  0017   (000023)   1002, 1260, 1603
0428    SELBF2  0010   (000016)   0608, 1001, 1256, 1284, 1330, 1560, 1618, 1621, 1746
0429    SNGDNF  0002   (000002)   0930, 0933, 1177, 1781
0430    SNSWDF  0008   (000008)   0609, 1158, 1233, 1407
0431    TRKOFS  0037   (000055)   0835, 0837
0432    US0     0021   (000033)   0922, 0949, 1048, 1052
0433    US1     0026   (000038)   0923, 0947, 1044, 1051, 1055
0434    US2     0025   (000037)   0924, 0943, 1045, 1054, 1058
0435    US3     0024   (000036)   0925, 0941, 1047, 1057
0436    WTOP1F  0009   (000009)   0602, 1145, 1598
0437    WTOP2F  0006   (000006)   1111, 1234, 1592, 1780
0438    WTRDMP  001F   (000031)   0998, 1119, 1247, 1409, 1604
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S Y M B O L S

DFF.LINE	NAME	ADDRESS	REFERENCED AT LINE NUMBER
0440	START1	0000	0440, 0453, 0454, 0457, 0467, 0477, 0478, 0479, 0480, 0481, 0482, 0483, 0484, 0494, 0495, 0496, 0497, 0498, 0499, 0508, 0509, 0511, 0513, 0514, 0516, 0530, 0531, 0532, 0533, 0534, 0547, 0557, 0558, 0559, 0560, 0561, 0562, 0563, 0564, 0565, 0566, 0567, 0568, 0569, 0570, 0571, 0572, 0589, 0590, 0593, 0594, 0597, 0598, 0616, 0617, 0618, 0619, 0623, 0624, 0626, 0627, 0630, 0631, 0632, 0633, 0634, 0635, 0636, 0637, 0638, 0641, 0643, 0645, 0648, 0650, 0663, 0675, 0685, 0697, 0707, 0711, 0715, 0724, 0727, 0731, 0732, 0737, 0740, 0741, 0750, 0751, 0761, 0769, 0770, 0771, 0772, 0773, 0787, 0790, 0794, 0799, 0808, 0809, 0818, 0819, 0821, 0824, 0825, 0827, 0829, 0836, 0844, 0847, 0858, 0859, 0862, 0876, 0878, 0880, 0883, 0887, 0890, 0898, 0903, 0905, 0906, 0914, 0916, 0917, 0919, 0920, 0926, 0932, 0938, 0940, 0942, 0944, 0946, 0948, 0950, 0974, 0978, 0988, 0990, 1006, 1007, 1008, 1010, 1028, 1039, 1040, 1041, 1049, 1050, 1053, 1056, 1059, 1060, 1063, 1065, 1069, 1072, 1076, 1079, 1082, 1097, 1112, 1113, 1114, 1115, 1123, 1124, 1125, 1126, 1127, 1128, 1129, 1132, 1133, 1134, 1135, 1137, 1138, 1139, 1140, 1141, 1143, 1144, 1147, 1148, 1149, 1150, 1151, 1153, 1154, 1155, 1159, 1160, 1161, 1163, 1165, 1169, 1170, 1171, 1172, 1174, 1175, 1178, 1179, 1180, 1181, 1183, 1192, 1193, 1204, 1205, 1208, 1213, 1231, 1232, 1238, 1240, 1241, 1242, 1250, 1251, 1254, 1258, 1259, 1261, 1262, 1272, 1273, 1276, 1277, 1279, 1292, 1294, 1296, 1297, 1299, 1300, 1305, 1337, 1339, 1340, 1342, 1346, 1348, 1360, 1365, 1370, 1372, 1377, 1381, 1385, 1386, 1387, 1394, 1408, 1412, 1415, 1416, 1418, 1423, 14255, 1426, 14227, 1434, 1436, 1445, 1447, 1449, 1452, 1453, 1454, 1476, 1477, 1479, 1482, 1483, 1484, 1489, 1493, 1494, 1495, 1496, 1498, 1500, 1501, 1502, 1503, 1504, 1509, 1511, 1518, 1519, 1520, 1522, 1523, 1524, 1525, 1526, 1527, 1528, 1530, 1535, 1536, 1537, 1539, 1541, 1542, 1544, 1546, 1547, 1548, 1551, 1552, 1555, 1561, 1580, 1583, 1584, 1586, 1587, 1589, 1590, 1593, 1594, 1596, 1597, 1600, 1601, 1602, 1605, 1608, 1611, 1614, 1617, 1623, 1624, 1626, 1628, 1629, 1630, 1635, 1636, 1637, 1639, 1641, 1643, 1644, 1647, 1648, 1649, 1651, 1652, 1653, 1655, 1656, 1657, 1666, 1671, 1673, 1674, 1676, 1677, 1678, 1683, 1684, 1685, 1686, 1687, 1689, 1691, 1692, 1694, 1697, 1702, 1703, 1705, 1706, 1707, 1708, 1710, 1711, 1712, 1716, 1719, 1720, 1722, 1725, 1727, 1728, 1729, 1730, 1732, 1733, 1734, 1736, 1737, 1740, 1741, 1742, 1745, 1753, 1754, 1755, 1756, 1757, 1758, 1760, 1770, 1771, 1772, 1774, 1775, 1776, 1777, 1787, 1789, 1790, 1791, 1792, 1793, 1794, 1795, 1796, 1797, 1798, 1799, 1800, 1801, 1802, 1803, 1805, 1806, 1807, 1808, 1809, 1810, 1811, 1812, 1813, 1814, 1817
0454	START2	0001	0453
0465	BANK	0005	0560
0466	FILEAD	0006	0561
0507	BSS1	0016	0497
0512	BSS6	001B	0509
0514	BSS8	001D	0508
0524	RTZS1	0020	0533, 0827, 1050, 1053, 1056, 1059
0532	RTZS8	0027	0530, 0534
0544	RTZS13	002C	0454
0588	WL1	0040	1561
0591	WL4	0043	0589
0593	WL6	0045	0590
0595	WL8	0047	0593

0597	WL10	0049	0594
0599	WL12	004B	0597
0602	WL14	004D	0598, 0740, 0862, 0906, 0978, 1169, 1192
0610	WL20	0055	0457, 0547, 0727
0614	WL24	0059	0942, 0944, 0948, 0950
0618	WL28	005D	0715
0620	WL30	005F	0616
0623	WL32	0061	0618
0625	WL34	0063	0617, 0623
0627	WL36	0065	0619, 0624
0628	WL37	0066	0626
0630	WL39	0068	0636, 0650, 0890, 1039, 1041
0633	WL42	006B	0631, 0643, 0645
0636	WL45	006E	0634
0638	WL46	0070	0632
0646	WL53	0077	0630, 0633, 0638, 0641
0649	REJECT	007A	0494, 0557, 0769, 0771, 0773, 0818, 0821, 0825, 0898, 0914, 0920
0651	WL58	007C	0648
0659	LDAD1	007D	0568
0671	RDFL1	0082	0498
0683	CWAS1	0087	0496
0693	LDBL1	008A	0564
0705	INRQ1	008F	0566
0712	INRQ7	0095	0707
0714	INRQ9	0097	0711
0723	BSCN1	0099	0565
0728	BSCN6	009E	0724
0732	BSCN10	00A2	1049
0739	BSCN16	00A8	0751
0742	BSCN19	00AB	0731
0744	BSCN21	00AD	0732, 0737
0750	BSCN27	00B3	0750
0759	FWAD1	00B5	0559
0769	STD1	00B8	0567
0772	STD4	00BB	0770
0774	STD6	00BD	0772
0782	STD14	00C4	1076, 1082, 1381
0790	STD22	00CC	0787
0793	STD25	00CF	0790
0798	STD29	00D3	0794
0801	STD31A	00D6	0799
0807	STD38	00DC	1060, 1193
0818	DF1	00E0	0558
0822	DF4	00E3	0819
0826	DF8	00E7	0824
0831	DF15	00EC	0829
0838	DF21A	00F3	0836, 1097
0846	DF26	00FA	0844
0849	DF28A	00FD	0847
0860	DF38	0108	0858
0863	DF40	010A	0859
0875	SCS2	010F	0499, 0903, 0905
0878	SCS6	0112	0876

0880	SCS9	0114	0878
0883	SCS12	0117	0880
0887	SCS15	011A	0883
0889	REPLY	011C	0467, 0495, 0511, 0513, 0514, 0516, 0531, 0627, 0663, 0675, 0685, 0697, 0761, 0926
0898	WFSC1	011E	0562
0904	WFSC7	0124	0887
0914	US01	0127	0563
0918	US6	012B	0916
0920	US8	012D	0917
0922	US10	012F	0919
0934	US23E	013A	0932
0943	US32	0143	0940
0945	US34	0145	0938
0949	US38	0149	0946
0959	TST11	014C	0569
0977	TST118	015D	1010
0986	TST41	015F	0572
0998	TST31	0164	0571
1003	TST34	0168	0988, 0990
1006	TST37	016B	1008
1009	TST39	016E	1006, 1007
1018	TDTS1	0170	0974
1019	TDTS2	0171	1028
1039	ATLD1	017D	0635
1042	ATLD4	0180	1040
1044	ATLD7	0182	0637
1050	ATLD12	0187	0741
1061	ATLD23	0192	0532
1065	ATLD27	0196	1063
1075	ATLD36	019F	1072, 1079
1077	ATLD38	01A1	1069
1083	ATLD44	01A7	1065
1107	TST21	01B7	0570
1126	TST219	01C9	1124
1128	TST221	01CB	1126
1130	TST223	01CD	1128
1134	TST226	01D0	1132
1136	TST228	01D2	1134
1140	TST232	01D6	1138
1145	TST237	01DB	1143
1149	TST241	01DF	1147
1154	TST245	01E3	1151
1161	TST252	01EA	1159
1166	TST257	01EF	1163
1167	TST258	01F0	1112, 1113, 1114, 1115, 1123, 1125, 1127, 1129, 1133, 1135, 1137, 1139, 1140, 1141, 1144, 1148 1149, 1150, 1153, 1154, 1155, 1160, 1161, 1170, 1171, 1172, 1174, 1175, 1179, 1180, 1181, 1789
1170	TST261	01F3	1165
1180	TST270	01FC	1178
1191	WLBU1	0200	0477, 0484, 0809, 1305, 1340, 1377, 1423, 1477, 1601, 1817
1201	DCBL1	0203	1476, 1509, 1583, 1586, 1589, 1600
1206	DCBL6	0208	1204, 1493, 1635
1209	DCBL9	020B	1205, 1213
1212	DCBL12	020E	1208

1231	SSS0A	0212	1238
1233	SSS1	0214	0483
1234	SSS2	0215	1602
1236	SSS3	0216	1479
1237	SSS4	0217	1300
1238	SSS5	0218	1231
1240	SSS6	0219	1241
1244	SSS9	021C	1240
1245	SSS11	021D	1482
1251	SSS16	0223	1251, 1580, 1594, 1671
1254	SSS19	0226	1254
1259	SSS24	022B	1261
1262	SSS27	022E	1262
1274	SSS39	0239	1272
1276	SSS41	023B	1277
1280	SSS45	023F	1273
1283	SSS48	0242	1279
1301	SSS61	0253	1259, 1276, 1292, 1299
1303	SSS63	0255	1296
1304	SSS64	0256	1294
1307	SSS67	0258	1258, 1297
1329	ADV0	025C	1522
1330	ADV1	025D	1452, 1705
1337	ADV4	0263	1337
1347	ADV13	026D	1339
1349	ADV15	026F	1346, 1385
1351	ADV19	0271	1342
1362	ADV29	027B	1360
1368	ADV35	0281	1365
1375	ADV42	0288	1386
1378	ADV45	028A	1370, 1372
1382	ADV49	028E	0808
1385	ADV51	0291	1387
1391	WRT74	0294	1652, 1653, 1655
1407	WAD1	0298	0482
1412	WAD4	029D	1453
1414	WAD5	029E	1418
1415	WAD6	029F	1416
1419	WAD10	02A3	1232, 1242, 1427, 1454
1424	WAD14	02A7	1348, 1415
1425	WAD15	02A8	1426
1428	WAD16	02AB	1425
1434	WAD22	02B1	1434
1436	WAD24	02B3	1436
1445	WAD30	02BB	1445
1447	WAD30B	02BD	1447
1449	WAD32	02BF	1449
1453	WAD36	02C3	1412
1474	READ1	02CA	0481
1475	READ2	02CB	0478
1478	READ5	02CE	1523
1483	READ10	02D3	1484
1490	READ16	02D9	1500

1494	READ20	02DD	1489
1495	READ21	02DE	1530
1499	READ25	02E2	1496
1500	READ26	02E3	1498
1501	READ27	02E4	1502, 1546, 1551
1503	READ29	02E6	1504
1505	READ31	02E8	1503
1524	READ48	02FA	1495
1531	READ54	0300	1525
1533	READ56	0302	1526, 1527, 1528, 1555
1536	READ59	0305	1494, 1537
1541	READ64	030A	1539, 1544, 1552
1545	READ68	030E	1535
1547	READ70	0310	1548
1552	READ74	0314	1542
1556	READ78	0318	1518
1558	READ80	031A	1511
1559	READ81	031B	1519, 1520, 1666
1580	WRT1	031E	1250
1592	WRT12	0329	1587, 1647
1595	WRT14	032C	0480
1597	WRT16	032E	0479
1598	WRT17	032F	1596
1602	WRT21	0333	1706
1603	WRT22	0334	1593
1608	WRT27	0339	1608
1611	WRT30	033C	1611
1614	WRT32	033E	1673
1615	WRT33	033F	1685
1616	WRT34	0340	1684
1623	WRT41	0347	1623
1626	WRT44	034A	1626, 1651
1627	WRT45	034B	1683
1631	WRT49	034F	1641
1636	WRT53	0353	1630
1637	WRT54	0354	1657
1641	WRT58	0358	1639
1645	WRT62	035C	1590
1646	WRT63	035D	1584
1648	WRT65	035F	1624, 1649
1650	WRT67	0361	1648
1652	WRT69	0363	1637
1661	WRT77	036B	1483, 1501, 1524, 1536, 1541, 1547, 1656, 1674, 1686
1663	WRT79	036D	1408, 1597, 1722, 1725, 1727
1665	WRT81	036F	1708
1667	WRT83	0371	1605
1674	WRT90	0378	1617, 1676
1679	WRT94	037C	1677
1680	WRT95	037D	1678
1684	WRT99	0381	1614
1686	WRT101	0383	1394, 1687, 1728, 1753
1689	WRT104	0386	1689
1691	WRT106	0388	1691, 1758

1692	WRT107	0389	1643, 1755
1694	WRT109	038B	1694
1697	WRT111	038D	1697
1698	WRT112	038E	1720
1707	WRT121	0397	1702, 1703, 1707
1709	WRT123	0399	1692
1710	WRT124	039A	1710
1711	WRT125	039B	1712
1713	WRT127	039D	1711
1721	WRT134	03A4	1719
1723	WRT136	03A6	1716
1728	WRT141	03AB	1628
1731	WRT144	03AE	1629
1733	WRT146	03B0	1636, 1644, 1734
1735	WRT148	03B2	1733
1736	WRT149	03B3	1736
1739	WRT151	03B5	1730, 1757, 1760
1740	WRT152	03B6	1740
1743	WRT155	03B9	1741
1744	WRT156	03BA	1729, 1742
1750	WRT162	03C0	1745
1752	WRT164	03C2	1732, 1737
1756	WRT168	03C6	1754, 1756
1770	T2U74	03CC	1183
1788	T2U91	03DD	1770, 1771, 1772, 1774, 1775, 1776, 1777, 1791, 1793, 1795, 1797, 1799, 1801, 1803, 1806, 1808 1810, 1812, 1814
1790	T2U93	03DF	1787
1792	T2U95	03E1	1790
1794	T2U97	03E3	1792
1796	T2U99	03E5	1794
1798	T2U101	03E7	1796
1800	T2U103	03E9	1798
1802	T2U105	03EB	1800
1805	T2U107	03ED	1802
1807	T2U109	03EF	1805
1809	T2U111	03F1	1807
1811	T2U113	03F3	1809
1813	T2U115	03F5	1811
1815	T2U117	03F7	1813

*** A L P H A B E T I C A L S O R T O F S Y M B O L S ***

ADRERR	0333	ADV0	1329	ADV1	1330	ADV13	1347	ADV15	1349	ADV19	1351	ADV29	1362	ADV35	1368	ADV4	1337
ADV42	1375	ADV45	1378	ADV49	1382	ADV51	1385	AINLS	0292	AINUS	0293	ALARMF	0391	ALARMJ	0334	ALDENF	0392
ALDENJ	0336	ALDFXD	0335	ALTFRC	0338	AOUTLD	0283	AOUTUD	0278	ATLD1	1039	ATLD12	1050	ATLD23	1061	ATLD27	1065
ATLD36	1075	ATLD38	1077	ATLD4	1042	ATLD44	1083	ATLD7	1044	AUTOLD	0337	AUXFF	0393	AUXJC	0339	BANK	0465
BANKD	0274	BF1ENB	0394	BF1F	0340	BF2F	0341	BF2LD	0284	BF2LS	0304	BF2UD	0285	BF2US	0305	BL1FF	0396
BL1JC	0343	BLZROF	0395	BLZROJ	0342	BMDL	0344	BMSB	0345	BREGD	0286	BREGS	0294	BSCN1	0723	BSCN10	0732
BSCN16	0739	BSCN19	0742	BSCN21	0744	BSCN27	0750	BSCN6	0728	BSS1	0507	BSS6	0512	BSS8	0514	BUSBSY	0346
BUSY	0397	CABIT0	0398	CASTRB	0399	CBITC	0320	CDMAER	0322	CNALU	0400	CNET	0321	CNTPRT	0401	COMP1	0404
COMP2	0405	COMPFF	0402	COMPJC	0347	COUT	0348	CRCERC	0312	CRCERJ	0349	CRCMOD	0406	CREQ	0314	CSFTRG	0407
CWALD	0279	CWALS	0300	CWAS1	0683	CWAUD	0281	CWAUL	0350	CWAUM	0352	CWAUS	0302	CWORD	0323	DCBL1	1201
DCBL12	1212	DCBL6	1206	DCBL9	1209	DF1	0818	DF15	0831	DF21A	0838	DF26	0846	DF28A	0849	DF38	0860
DF4	0822	DF40	0863	DF8	0826	DKWTPT	0354	DMAREQ	0310	DMWRPT	0408	DSKERR	0355	EGWG	0409	ENBDB	0410
ENBNED	0411	ENWDSY	0412	EOP	0413	EQUAL	0356	FILEAD	0466	FRCBUS	0414	FRINXC	0315	FRINXJ	0357	FRSTDT	0358
FWAD1	0759	HFWRD	0359	HS1	0415	HS2	0416	I	0000	INDEX	0360	INRQ1	0705	INRQ7	0712	INRQ9	0714
INTRSP	0417	JGRP9	0418	LDAD1	0659	LDBL1	0693	LSTDT	0361	MODE0	0251	MODE1	0252	MODE2	0253	MODE3	0254
MODE4	0255	MODE5	0256	MODE6	0258	MODE7	0259	MODE8	0260	MODE9	0261	MODEA	0262	MODEB	0264	MODEC	0265
MODED	0266	MODEE	0267	MODEF	0268	MSW1	0362	MSW2	0363	NOCOMP	0364	NU	0272	ONBUSF	0419	ONBUSJ	0366
ONCYL	0367	ONOFLN	0368	PARERR	0369	PCD	0276	PCS	0296	PRGPRT	0371	PRIOR	0420	PRTFLT	0370	QS	0295
RAMADD	0273	RAMD	0275	RAMS	0290	RDFL1	0671	RDGATE	0421	RDZERO	0316	READ1	1474	READ10	1483	READ16	1490
READ2	1475	READ20	1494	READ21	1495	READ25	1499	READ26	1500	READ27	1501	READ29	1503	READ31	1505	READ48	1524
READ5	1478	READ54	1531	READ56	1533	READ59	1536	READ64	1541	READ68	1545	READ70	1547	READ74	1552	READ78	1556
READ80	1558	READ81	1559	REJ	0309	REJECT	0649	REPLY	0889	RMBNKS	0422	RMEXEC	0372	RPLY	0311	RQBUS1	0423
RQBUS2	0424	RTZS	0425	RTZS1	0524	RTZS13	0544	RTZS8	0532	RWMOD	0426	SBF1F	0318	SBF2F	0319	SCS12	0883
SCS15	0887	SCS2	0875	SCS6	0878	SCS9	0880	SECTOR	0374	SEEKER	0373	SELBF1	0427	SELBF2	0428	SKCMP0	0376
SKCMP1	0377	SKCMP2	0378	SKCMP3	0379	SNGDNF	0429	SNGDNJ	0375	SNSWDF	0430	SNSWDJ	0380	SSS0A	1231	SSS1	1233
SSS11	1245	SSS16	1251	SSS19	1254	SSS2	1234	SSS24	1259	SSS27	1262	SSS3	1236	SSS39	1274	SSS4	1237
SSS41	1276	SSS45	1280	SSS48	1283	SSS5	1238	SSS6	1240	SSS61	1301	SSS63	1303	SSS64	1304	SSS67	1307
SSS9	1244	START1	0440	START2	0454	STD1	0769	STD14	0782	STD22	0790	STD25	0793	STD29	0798	STD31A	0801
STD38	0807	STD4	0772	STD6	0774	T2U101	1798	T2U103	1800	T2U105	1802	T2U107	1805	T2U109	1807	T2U111	1809
T2U113	1811	T2U115	1813	T2U117	1815	T2U74	1770	T2U91	1788	T2U93	1790	T2U95	1792	T2U97	1794	T2U99	1796
TDTS1	1018	TDTS2	1019	TRKOFS	0431	TST11	0959	TST118	0977	TST21	1107	TST219	1126	TST221	1128	TST223	1130
TST226	1134	TST228	1136	TST232	1140	TST237	1145	TST241	1149	TST245	1154	TST252	1161	TST257	1166	TST258	1167
TST261	1170	TST270	1180	TST31	0998	TST34	1003	TST37	1006	TST39	1009	TST41	0986	UNRDY	0381	UNTPRT	0382
US0	0432	US01	0914	US1	0433	US10	0922	US2	0434	US23E	0934	US3	0435	US32	0943	US34	0945
US38	0949	US6	0918	US8	0920	USNGDN	0383	WAD1	1407	WAD10	1419	WAD14	1424	WAD15	1425	WAD16	1428
WAD22	1434	WAD24	1436	WAD30	1445	WAD308	1447	WAD32	1449	WAD36	1453	WAD4	1412	WAD5	1414	WAD6	1415
WCD	0277	WCEMPT	0384	WCS	0291	WFSC1	0898	WFSC7	0904	WL1	0588	WL10	0597	WL12	0599	WL14	0602
WL20	0610	WL24	0614	WL28	0618	WL30	0620	WL32	0623	WL34	0625	WL36	0627	WL37	0628	WL39	0630
WL4	0591	WL42	0633	WL45	0636	WL46	0638	WL53	0646	WL58	0651	WL6	0593	WL8	0595	WLBU1	1191
WORD	0385	WRT1	1580	WRT101	1686	WRT104	1689	WRT106	1691	WRT107	1692	WRT109	1694	WRT111	1697	WRT112	1698
WRT12	1592	WRT121	1707	WRT123	1709	WRT124	1710	WRT125	1711	WRT127	1713	WRT134	1721	WRT136	1723	WRT14	1595
WRT141	1728	WRT144	1731	WRT146	1733	WRT148	1735	WRT149	1736	WRT151	1739	WRT152	1740	WRT155	1743	WRT156	1744
WRT16	1597	WRT162	1750	WRT164	1752	WRT168	1756	WRT17	1598	WRT21	1602	WRT22	1603	WRT27	1608	WRT30	1611
WRT32	1614	WRT33	1615	WRT34	1616	WRT41	1623	WRT44	1626	WRT45	1627	WRT49	1631	WRT53	1636	WRT54	1637
WRT58	1641	WRT62	1645	WRT63	1646	WRT65	1648	WRT67	1650	WRT69	1652	WRT74	1391	WRT77	1661	WRT79	1663
WRT81	1665	WRT83	1667	WRT90	1674	WRT94	1679	WRT95	1680	WRT99	1684	WTOP1F	0436	WTOP1J	0386	WTOP2F	0437
WTOP2J	0387	WTRDMP	0438														

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Hardware Reference/Maintenance Manual

PUBLICATION NO. 89600661 REVISION A

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